A CMOS Compatible III-V-on-300 mm Si Technology for Future High-speed Communication Systems: Challenges and Possibilities

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Abstract—**III-V semiconductor-based devices, in particular InP heterojunction bipolar transistors, are a strong contender for next-generation high-speed communication systems. In this paper, we present motivation for the upscaling of III-V technology on to 300 mm Si platforms. A comparison of various options for such III-V on Si technology is described. The challenges in the way to achieve its integration into existing CMOS platform and possibilities to overcome them are shown. We describe imec's path to demonstrate a CMOS compatible III-V-on-300 mm Si technology with the most recent results.**

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Index Terms—**III-V, HBT, 6G, InP, III-V on Si**

I. INTRODUCTION

THE integration of III-V compound semiconductor-based heterojunction bipolar transistors (HBTs) on Si substrates has been identified as one of the promising routes to enable hybrid III-V/CMOS technology for future RF applications [1–3]. GaAs/InGaP HBTs grown on small size native GaAs substrates are already being used in power amplifiers in mobile phones due to several advantages over other possible material combinations. However, future technologies for high-speed communication applications, such as 6G, would require:

- Better performance from such devices in f_t, f_{max}, P_{out}, and PAE
- Large volume production at significantly lower cost
- Flexibility in circuit design
- Smaller chip footprint [1,2].

All these requirements can be achieved by the monolithic growth of III-V materials

on the Si substrate and its integration with state-of-the-art CMOS back-end-of-the-line process for routing complex control signals. As far as III-V growth on Si substrate is concerned, several techniques have been explored; examples are strain relaxed buffer (SRB) layers on Si wafers [4], GaAs grown on Si/SiGe-based compositionally graded buffers [5], confined epitaxial lateral overgrowth (CELO) [6], and aspect ratio trapping (ART) inside the narrow trenches [7]. A review of various monolithic integration approaches is given in [8]. In particular, for RF applications, silicon on lattice engineered substrates (SOLES) [9] have been used to demonstrate InP HBTs co-integrated with CMOS but has the disadvantage of requiring expensive starting substrates and very thick buffer layers to grade to the InP lattice constant, which contradicts with cost and complexity requirements of such future technologies. It is imperative, then, that in order to minimize the complexity and cost of a hybrid CMOS/III-V technology, standard Si substrates should be used.

Furthermore, with ever-growing requirement for larger bandwidths for mm-wave applications, InP-based HBTs are gaining importance [10]. It is then obvious that a cost-effective hybrid CMOS/III-V technology on a standard 300 mm Si substrate, which can be extended to InP-based material system, would be highly desirable.

In this work, we present a comparison of various options for a hybrid III-V/CMOS on Si technology. Various challenges in the way to achieve such an integration into existing CMOS platform and possibilities to overcome them are shown. Furthermore, we report imec's path to demonstrate a CMOS compatible III-V-on-300 mm Si technology consolidated with the most recent electrical characterization results of InP HBTs.

II. III-V ON SI SUBSTRATES: OPTIONS AND CHALLENGES

One of the major challenges related to the integration of III-V materials on Si substrates is the large mismatch in lattice constant as compared to Si (4% for GaAs and 8% for InP and InGaAs) and thermal expansion coefficient, which creates a large number of relaxation defects in the semiconductor layers [8]. These defects have been shown to severely limit the electrical performance of devices [6]. This has led the research on the techniques to integrate III-V materials on Si to diversify into two broad categories: heterogeneous integration, where the challenge is circumvented by directly bonding a high quality III-V layer or substrate to the Si substrate, and monolithic integration, where III-V material is directly grown on Si. In both categories, there are several integration options among which, in the following section, the most promising techniques are described in more detail.

A. Heterogeneous Integration

The heterogeneous integration techniques, an example of which is shown in Figure 1, involve growing a III-V device stack on native III-V (GaAs or InP) substrate, cleaving the device wafers into square tiles, and transferring these tiles by the pick-and-place technique directly onto the large-diameter target Si wafer by a bonding process [12,13]. The sequence of stack growth, cleaving, and bonding might change depending on the technique. The bonding process can be a direct III-V to Si bonding or a dielectric–dielectric layer bonding, such as silicon oxide or silicon nitride. Both techniques suffer from a potential challenge of maintaining highly smooth surface free of small particles. Adhesive bonding involving an adhesive material, such as epoxy,

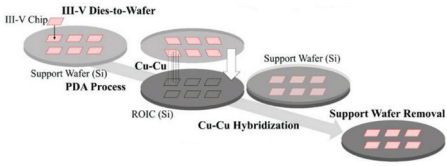

Fig. 1. An example of heterogenous integration for visible-SWIR image sensor with read-out integrated circuit (ROIC). III-V chip can either be just a diced native substrate or a die with already fabricated device [13]. Bonding process can consist of Cu–Cu or oxide–oxide hybrid bonding.

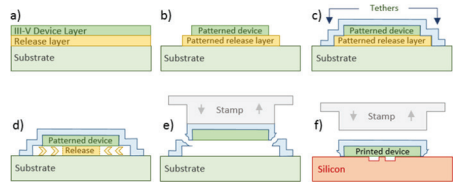

Fig. 2. The μ-transfer printing process. (a) and (b) The definition of the III-V device on the III-V source wafer. (c) and (d) The structures are encapsulated and the release layer is selectively etched. (e) The use of a stamp to pick-up arrays of III-V devices from the source wafer. (f) Print them onto the silicon photonic target wafer, after which the encapsulation is removed and the III-V devices are electrically contacted on a wafer-scale [16].

polyimide, or benzo-cyclobutene has also been used for this purpose, with the advantage of not requiring strict surface cleanliness or smoothness requirements. Another challenge in using this technique is to maintain the stability of the tile/wafer interface during the removal of the InP substrate or subsequent process steps, as the grinding/wet etching process may cause stress and lead to cracks in the III-V device layer. Corners of the tiles are particularly vulnerable during this process step. In the case of adhesive bonding, the temperature range of the bonding material limits the thermal budget of all subsequent process steps. Nevertheless, some of these approaches do show promise in circumventing some of the above issues.

Micro-transfer printing is one such heterogeneous integration approach for transferring partly or fully processed III-V devices to Si-based wafers (Figure 2) [14–16]. It requires the growth of a modified device stack on a release layer; for InP, for example, the release layer may consist of InAlAs. Before the transfer, the InP substrates undergo several process steps following the epitaxial growth of the HBT device stack. In these process steps, device mesas are created and the release layer is selectively removed by wet etch resulting in a device layer attached to the substrate only by polymer tether structures. Using a polymer stamp, the devices are then picked by breaking the tether structures and transferred to the target wafer. This technique is limited by the possible lateral material removal of the release layer. Furthermore, there are concerns regarding the possibility of yield issues due to fragments of the broken tethers and process instabilities. The choice of the adhesive bonding layer is also not straightforward to ensure a stable bonding interface during device processing. Although the accuracy of the printing tools has shown improvements recently, it is still challenging to minimize particle contamination during multiple pick-and-place cycles.

Another promising heterogeneous integration approach is to transfer only a thin InP film to the target Si wafer. This InP film is then used as a starting surface for the epitaxial growth of the device stack. [17]. Such engineered substrates are also referred as InP on silicon (InPOSi). One of the main challenges in such a transfer is related to the release of this thin InP layer from native substrate. One approach is the bonding of a bulk InP substrate, including a top thin InP and etch-stop sacrificial layer, on a Si wafer, followed by a backside wet etching of the full InP bulk material [17]. In such a case, not

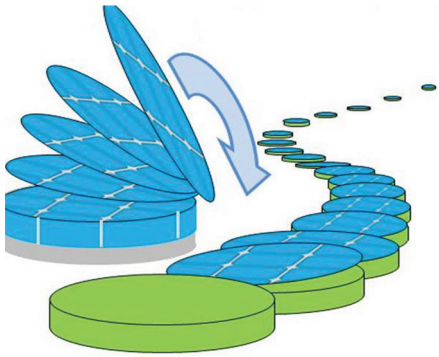

Fig. 3. Simplified sketch of the production of tiled 200/300 mm InPOSi wafers [18].

only the small size of the native InP substrates (4”) poses a problem, but the recycling out of the etchant waste, which also includes precious InP material, may also be challenging.

A more cost-effective approach for transferring InP films is described by Ghyselen et al. [18] based on the Smart Cut™ technology initially introduced by Soitec for the fabrication of SOI wafers (Figure 3). In such a process, an InP donor wafer, a Si target wafer, or both are covered with an oxide layer. The InP substrate is then subjected to hydrogen ion implantation, forming a buried layer of microcavities at a defined depth. After the wafer-to-wafer bonding, a thermal treatment is applied to split off the InP substrate at the buried layer and to strengthen the covalent bonds along the bonding interface of the achieved InPOSi wafer. This process leads to a thin InP film on top of the target oxidized Si wafer while circumventing the issues with wet-etch-based substrate removal and saving InP material from going to waste. Although it is still challenging to upscale this technique to wafer sizes of 200–300 mm, there have been some developments in this regard where a 200mm InP-tiles-based pseudo-donor wafer is first created using traditional transfer approaches, which is then used as a native substrate for transfer as described above [18]. Such native pseudo-donor wafers can be used for several cycles of transfer improving the reusability of the donor substrate. A challenge using this technique is related to post-bonding epitaxial growth temperature. As the wafer-to-wafer bonding process is performed at room temperature, heating up to the growth temperature (typically > 550 °C) induces compressive strain in the InP film because of the larger thermal expansion coefficient of III-V materials compared to the one of Si. Consequently, innovative strain management techniques are required for the III-V growth on InPOSi wafers to prevent the formation of misfit defects inside the HBT device stack.

While all the above techniques show some promise in large-scale integration, the cost of InP substrates to be required is a very vital factor to consider in mass production. While a larger market for InP substrates may lead to lower substrate costs, scarcity may result in price hikes. In this respect, it may be interesting to recycle waste products generated during InP grinding, for instance. The sustainability and conversion efficiency of such recycling is a major aspect that should not be ignored in the assessment of upscaling. The reduction of the environmental impact should be a strong driving force in the development of future technologies and requires dedicated life-cycle assessments.

B. Monolithic Integration

Given the above-mentioned constraints regarding material cost and sustainability, the most cost-effective approach for integrating III-V materials with Si substrates seems to be the direct monolithic deposition, eliminating the need for InP substrates. However, the mismatch in

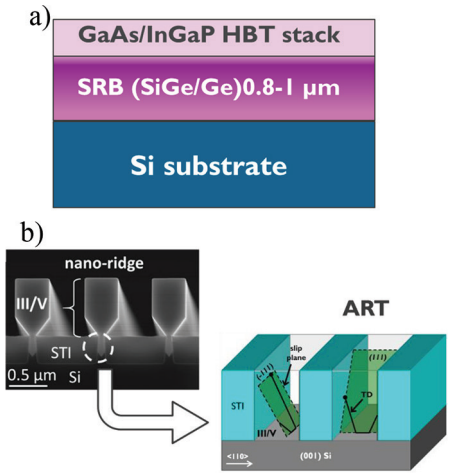

Fig. 4. (a) An example of SRB-based growth of III-V on Si substrate using a thick buffer layer. (b) Cross-sectional SEM image of an NR array. (b) Aspect ratio trapping (ART), where defects are trapped in narrow trenches [19].

lattice constants and thermal expansion coefficients between Si and III-V materials results in the formation of relaxation defects, which adversely affect the performance of HBT devices. The growth of SRB prior to the deposition of the device layers allows to reduce the defect density in HBTs (Figure 4a). In this context, various strategies have been developed to eliminate relaxation defects, including the use of strained layer superlattices as a defect filter, the application of composition gradients, and the use of cyclic annealing treatments. Nevertheless, a low defect density at the buffer surface requires the growth of a several µm thick SRB, which can cause new problems with wafer warpage and crack formation in the III-V layer (9).

Selective area growth (SAG) is an alternative monolithic integration approach that circumvents the issues related to blanket layer growth [6,7]. This method, CELO as an example, involves patterning an oxide layer on top of a Si wafer to expose the Si surface through confined openings. The III-V material is then epitaxially deposited inside these openings under growth conditions that promote selective growth. A high aspect ratio (depth divided by the width) of the patterned openings helps to reduce defects efficiently within a thin layer deposition, as threading dislocations and planar defects (PDs) tend to be trapped at the sidewalls [7]. However, an effective ART of defects inside the openings is accompanied by a small III-V volume confined by the pattern dimension, which poses challenges in realizing an HBT for useful power amplification (9).

Nano-ridge (NR) engineering is a novel integration technique that provides a solution for increasing the volume of III-V material (Figure 4b) [9,19]. It builds upon SAG and ART and involves the application of Si wafers with a narrow trench pattern, where each trench bottom is formed by two {111} facets creating a V-shape, which impedes the formation of anti-phase disorder in the III-V material. A high aspect ratio (>3) of the trenches ensures efficient defect trapping near the III-V/Si interface. The growth is performed by metal-organic vapor phase epitaxy (MOVPE). Once the trenches are filled with III-V material, growth continues out of the trenches to create a large NR above the oxide mask with an increased volume of III-V material. Manipulating the growth rate hierarchy on the different NR facets through adjusting the MOVPE conditions offers the possibility to engineer the shape of the NR. The advantages of using NRE for scaling up the InP technology are evident due to the monolithic III-V integration to Si, which removes the need for InP substrates, thereby reducing cost and potentially enhancing sustainability. The III-V device deposition can be done directly on large-diameter substrates in a 200/300 mm CMOS foundry, without

the need of any complicated III-V layer transfer or bonding processes, resulting in a lower risk of particle contamination and yield loss. The application of SAG on patterned wafers makes the growth of thick SRBs unnecessary and enables advanced device scaling and circuit design since the mask layout determines the III-V device distribution throughout the patterned Si wafer. This approach is detailed in the next section.

III. III-V-ON-300 MM SI SUBSTRATE AT IMEC

A. Monolithic Integration using Nano-Ridge Engineering

To integrate III-V materials on 200/300 mm Si substrates, imec is researching on both heterogeneous and monolithic approaches. In the monolithic approach, imec has developed a fabrication process based on NRE, which selectively grows the III-V material in pre-patterned structures or trenches in the Si (see Figure 5).

These high-aspect-ratio trenches are very effective in trapping the defects in the narrow bottom part and growing high-quality, low defect material out of the trench. In addition to a high-aspect-ratio trench to capture defects, a second silicon oxide pattern is added to the original trench pattern, which has the same pitch but a wider opening. After filling the first oxide trench on top of the Si substrate, the MOVPE parameters are adjusted to promote lateral broadening of the NR until it reaches the sidewalls of the second oxide pattern. In this way, the collector material of the HBT is in contact with the oxide sidewall, and subsequent p- and n-doped device layers only grow on the (001) surface without any sidewall deposition. The related illustration is shown in Figure 5c. The successful implementation of this integration concept for a GaAs-based

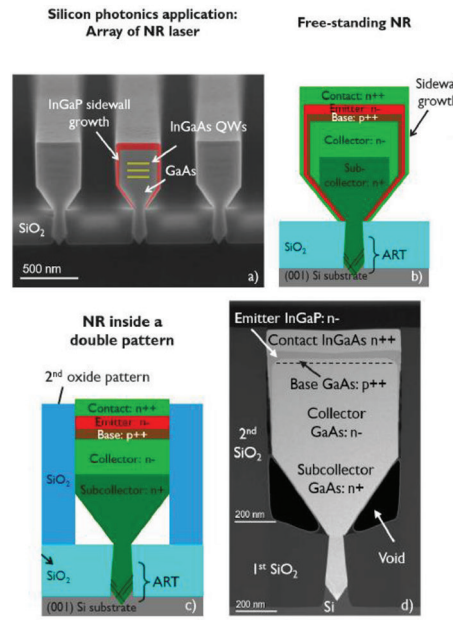

Fig. 5. (a) Cross-sectional SEM image of an NR laser array. (b) The impact of sidewall deposition when an HBT device stack is deposited on a free-standing NR. (c) A second oxide pattern on the first prevents sidewall growth. (d) HAADF-STEM (high-angle annular dark-field scanning transmission electron microscopy) image of a GaAs-based NR HBT [19].

HBT structure grown on a double patterned 300 mm Si wafer is shown in Figure 5d. The threading dislocation density (TDD) at the surface of NRs deposited in narrow trenches has been reported for GaAs NRs to be below 3 × 106 cm−2 based on electron channeling contrast imaging (ECCI) [19]. This defect density value is limited by the ECCI inspection area; therefore, the actual TDD could be even lower for the GaAs NRs. In the TEM investigation of the NR HBT device stack, no indication of any misfit or threading dislocations was found outside the STI trench. All mismatch-induced defects were restricted inside the trench and confined close to the GaAs/Si interface by ART. The complete III-V device stack in the second oxide is free of TDs. Only PDs

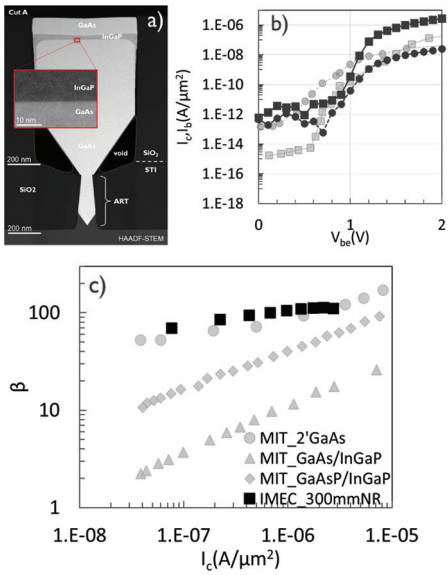

Fig. 6. (a) HAADF-STEM of GaAs/InGaP HBT stack after epitaxial deposition on 300 mm (100) silicon substrate along and across a nano-ridge. (b) A comparison of electrical characterization (Gummel plot) of the devices fabricated in this work with that of ref. [6]. (c) A comparison of DC current gain, β, of our HBT with that of ref. [6] with respect to collector current [20].

such as stacking faults and micro-twins could be found in the device stacks laying in a {111} plane perpendicular to the trench. The density of 0.5–0.9 μm^{-1} (PD per NR length) is slightly higher as it was observed for GaAs NRs deposited on single oxide pattern [19]. However, as PDs do not involve either open crystal bonds or a pronounced strain field, we expect less impact on the device performance in comparison to dislocation defects.

Initially, HBT devices on such stacks were demonstrated to be fabricated on small coupons taken from these 300 mm wafers (Figure 6) [20–22]. The ideality factors of NRE-based emitter-base and base-collector diodes were ~1.2 and 1.4, respectively, indicating the good quality of EB and BC junctions. An HBT device showed a peak DC gain, β, of 112 at

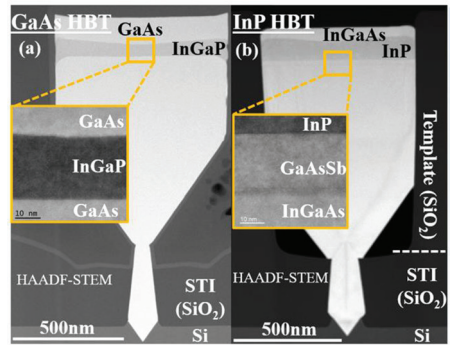

Fig. 7. HAADF-STEM pictures of (a) GaAs and (b) InP HBT stacks on 300 mm Si substrate across a single nano-ridge (NR) showing good device layers interface quality [23].

V_{be} = 2 V. A breakdown voltage, BV_{cbo}, of 10 V was also measured on this device. The quality of the layer interfaces, verified using electrical characterization, was found to be similar to the same stack grown on high-quality GaAs substrates. Furthermore, HBTs fabricated on this stack showed an electrical performance considerably better than GaAs(P) devices fabricated on a Si substrate with SRB layers, without any need to grow thick (>1–10 μm) buffer layers.

Recently, imec demonstrated the first monolithic integration of III-V HBTs on 300 mm Si substrate using standard fabrication in a CMOS pilot line for both GaAs and InP HBTs (Figure 7) [23]. The fabrication for both material systems was done completely in a 300 mm CMOS pilot line at imec with excellent electrical characterization results with low across-the-wafer and wafer-to-wafer non-uniformity (Figure 8). The ideality factors of collector and base current for GaAs HBTs are ~1.0 and 1.45, respectively (as compared to ~1.02 and ~1.6 on GaAs substrate), indicating on the effectiveness of the integration in maintaining the good quality of hetero interfaces. A good DC current gain, β_{GaAs} ~ 40 and β_{InP} ~ 7, and ON

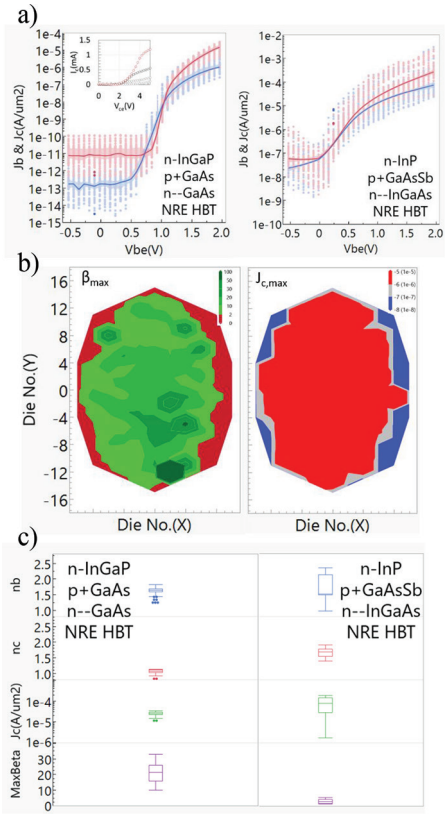

Fig. 8. (a) Gummel plots of HBTs fabricated on GaAs and InP NRE material stack. The output characteristic of GaAs HBT is also shown in the inset. (b) Across wafer variation of DC current gain and maximum collector current of a GaAs NRE HBT wafer. (c) Key DC parameters variation of GaAs (left) and InP (right) NRE HBTs [23].

current density, $J_{c,GaAs} \sim 6 \times 10^{-5}$ A/μm², $J_{c,InP} \sim 3 \times 10^{-4}$ A/μm² is observed for GaAs and InP devices, respectively. Moreover, a BV_{CEO} and BV_{CBO} of ~8 and ~13 V, respectively, are measured on GaAs NRE HBTs. These values, although not state-of-the-art, are comparable to similar devices made on 2" native substrates. By demonstrating it for two different III-V material systems, GaAs and InP, imec showed this technology's flexibility to cover several III-V based application domains ranging from FR3, 6G, and optical I/O systems.

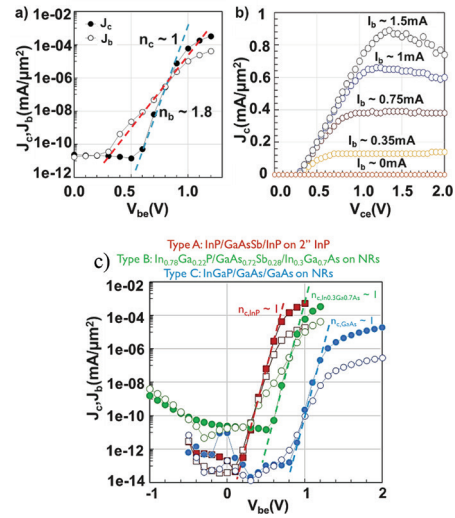

Fig. 9. (a) Transfer and (b) output characteristics of an NR-HBT fabricated on $In_{0.78}Ga_{0.22}P/GaAs_{0.72}Sb_{0.28}/In_{0.30}Ga_{0.70}As$ stack. (c) A comparison of the Gummel plots of HBTs fabricated on three different III-V material systems to illustrate the improvement of on current in $In_{0.3}Ga_{0.7}As$ NR HBTs as compared to GaAs NR HBTs [24].

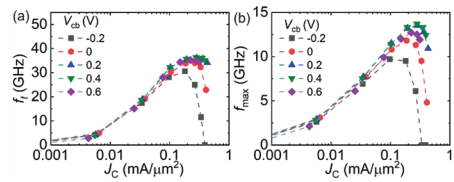

Fig. 10. (a) f_t and (b) f_{max} for a device with W_E: 5 μm and 55 nano-ridges (L_E: 44 μm) as functions of current density J_C. At $V_{cb} = 0.4$ V, extracted peak f_t is ~36 GHz and peak f_{max} is 13.7 GHz [24].

In addition, imec also demonstrated, recently, an example of this versatility by fabricating an NRE-based Ga-rich $In_{0.78}Ga_{0.22}P/GaAs_{0.72}Sb_{0.28}/In_{0.3}Ga_{0.7}As$ HBTs on 300 mm Si substrates, which can achieve better performance as compared to InGaP/GaAs HBTs FR-2 and FR-3 5G applications as shown by the DC and RF electrical performance of these devices (Figures 9 and 10) [24]. The ideality factors of collector and base currents are ~1.0 and ~1.8, respectively. The device

showed a DC current gain of ~10 at V_{be} = 1.2 V and breakdown voltages, BV_{CEO} and BV_{CBO}, of ~ 2.5 and 4.5 V, respectively. At V_{cb} = 0.4 V, extracted peak f_t is ~36 GHz and peak f_{max} is 13.7 GHz for a device with emitter width W_E: 5 µm and with 55 NRs (L_E: 55 × 0.8 µm = 44 µm).B. Heterogeneous Integration using InPoSi

Due to InPoSi's capability to upscale to large wafer sizes without any issues of release layer removal and its advantages related to sustainability and reusability, imec is also investigating InPoSi's application in developing a III-V on Si technology. In this direction, HBT stack is grown on a 4" InPoSi substrate and on a 4" InP substrate (for comparison) using MOCVD. The InP layer bonded onto the SOI wafer to create the 4" InPoSi wafer was taken from a 4" InP substrate from the same batch as the 4" InP substrate used here for comparison. The RMS surface roughness of the HBT stack on InPoSi, measured using AFM, is observed to be similar to that on InP substrate (~0.13 nm) indicating good epitaxial growth. Large-area HBT devices fabricated on the above stack showed good DC performance. The ideality factors of collector and base currents were ~1.0 and 1.7 (as compared to ~1.0 and 1.3 for the 4" reference InP substrate) respectively indicating the good quality of hetero-interfaces. An HBT device showed a peak DC gain, β, of ~100 is observed at Vbe = 1 V. The breakdown voltages, BVceo and BVcbo, of 3.5 and 5.5 V, respectively, were also measured on this device. A comparison of the DC performance of HBTs on InPoSi and InP substrate is shown in Figures 11 and 12. Further investigation on the RF performance of HBTs on InPoSi is underway. Nevertheless, negligible differences in the performance of HBTs on InPoSi substrate from that on native substrate points to promising future of this technique in the development of III-V on Si technology.

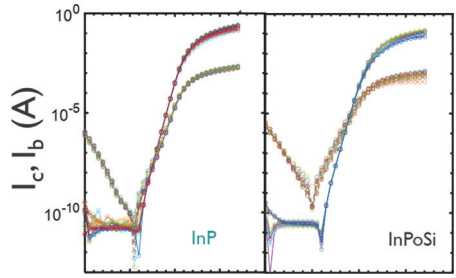

Fig. 11. Transfer characteristics of a InP/GaAsSb/InP HBT fabricated on InP (left) and InPoSi (right) substrates. Except for the difference in base current ideality factor and leakage, ON state performances of both are quite similar and good.

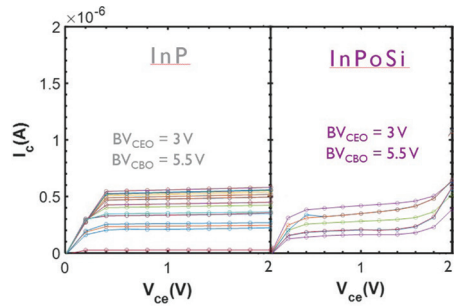

Fig. 12. Output characteristics of an InP/GaAsSb/InP HBT fabricated on InP (left) and InPoSi (right) substrates for the same base currents. Note the slight difference in the output current.

V. CONCLUSION

The cost-efficient and sustainable integration of III-V on Si is critical for the success of future high-speed communication systems. Different approaches have been reviewed, with a special emphasis on imec's recent developments, which are at the forefront of the research to achieve a hybrid III-V/CMOS technology. Compared to the other approaches, NR engineering (for monolithic approach) and InPoSi (for heterogeneous integration) look promising. While CMOS is compatible, both

approaches highlighted excellent DC and RF performance of HBTs fabricated on a variety of III-V material systems.

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