Ka-Band GaN-on-SiC Power Amplifier for High EIRP Satellite Phased Antenna Array

Francesco Manni, Paolo Colantonio, Rocco Giofrè, Ernesto Limiti, Patrick Ettore Longhi, Steven Caicedo Mejillones, Stefano Moscato, and Alessandro Fonte

Abstract—**This work presents a transmitter-only phased antenna array architecture for Ka-band satellite applications, specifically from 25.5 to 27 GHz. The design targets an optimum design point among the number of elements, the output power from each transmitter, the antenna EIRP, and its steering capabilities. The core of the system relies on a custom designed power amplifier based on AlGaN/GaN epitaxy grown on 4-inch SiC substrate featuring 20 dB of gain and 28 dBm of saturated power. The antenna array front-end is envisaged as a lattice of 64 hollow metallic horns, spaced by 16 mm from each other. The amplifiers paired with the antenna array targets 70 dBm of EIRP, even considering the maximum beamsteering configuration of ±20°. The proposed concept highlights the flexibility in targeting different power levels, antenna gain, and steering capabilities to finally address a large number of use-cases.**

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Index Terms—**Antenna array, Ka-band, phased array, power amplifier, mmWave**

I. INTRODUCTION

AMONG the characteristics of a transmitting phased antenna array (PAA), the effective isotropic radiated power (EIRP) is one of the most important. In fact, the received signal-to-noise ratio is mostly affected by the EIRP at the transmitter side of the link. However, the maximization of both the amount of radiated power and the antenna gain implies trade-offs, which can limit the applicability of the array system itself. For example, an enhancement of the antenna gain leads to a cumbersome reflector or a large array footprint, which can be an issue for both terrestrial and flying transceivers.

The millimeter wave (mmWave) front-end for transmitters on-board to satellites and spacecrafts is generally demanded to a travelling wave tube amplifier paired with a low gain antenna element. The aforementioned amplification stage has excellent performance in terms of power handling, linearity, efficiency, and reliability, proven since decades. However, motors and actuators are generally exploited to allow a fine compensation of the beam direction with disadvantages in

terms of on-board mechanical hindrances, weight, reliability, and costs.

Phased antenna array (PAA) is proven to be the solution since it is fully customizable [1–4], scalable in EIRP and frequency, and can be even flat, overcoming the adoption of standard parabolas or isoflux antennas. Basic elements can be fed or clustered, balancing EIRP and steering capabilities [5].

However, PAAs exhibit a main drawback in use-cases where high EIRP is required and the available power supply is limited. The adoption of a large number of radio frequency (RF)-integrated circuits leads to a significant amount of power drawn from the system. The main responsible is clearly the final amplification stage where the power added efficiency (PAE) is the main feature to be taken into account in PAA systems. Not less important, PAE tends to drop for higher frequencies, but in modern systems, the trend is to push the connectivity in the mmWave range to exploit wider channels and, in turn, higher data throughput at a given constellation scheme [6–8].

Power amplification stages based on GaN on SiC have been proved to be the perfect candidate when the power efficiency is paramount, even above the standard microwave frequency bands [9]. The envisaged architecture of PAA perfectly suits the adoption of power amplification stages based on GaN since it opens the possibility to keep high the output power level without an exponential growth of the overall power consumption of the system.

The concept introduced with this manuscript is named ESKaA, which stands for "Electronically Steerable Ka-band Antenna." ESKaA exploits a custom-designed GaN-on-SiC PA and a uniform lattice of 64 horns as radiating elements where the main features are reported in Table I. This manuscript is organized in five sections: Section II introduces the most important trade-off in the phased array design, Section III describes the design of the PA, and Sections IV and V show the system architecture and the antenna performance, respectively. Section VI concludes the paper.

TABLE 1.
SPECIFICATIONS BASED ON THE IDENTIFIED USE-CASE.

Specification	
Operational net bandwidth	25.5–27 GHz
Polarization	Circular
EIRP (guaranteed at max scan angle)	>70 dBm
Scan angle (free from grating lobes)	±20°
DC power consumption	<120 W
Dimensions (max footprint)	200 × 200 mm^2

II. TRADE-OFF IN THE PHASED ANTENNA ARRAY DESIGN

This section describes an effective way to preliminarily estimate the array order N and the recommended output power P_{TX} on each amplifier. The method considers, as input, the required EIRP and the gain of the basic radiating element. To do so, the starting point is the definition of EIRP in dBm, which can be calculated by the following equation:

$$EIRP = 10\log_{10}(N) + G + 10\log_{10}(N) + \mathrm{P}_{TX}$$

where G is the gain of the base-block element in decibel and P_{TX} is expressed in dBm. Here it is assumed that each base-block antenna is fed by a single active component. Another assumption is that the base antenna is a circularly polarized horn with 12 dBi of gain. Considering the above-mentioned assumptions, Figure 1 shows a trade-off between P_{TX}, N, and EIRP. The more EIRP is needed, the greater the array order or output power

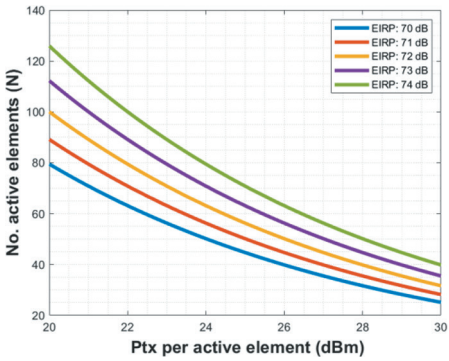

Fig. 1. EIRP, N, P_{TX} trade-offs in the considered phased array antenna architecture.

TABLE 2.
TRADE-OFF IN TARGET EIRP (G = 12).

EIRP (dBm) =	**70**	**71**	**72**	**73**	**74**
P_{TX} for N = 7 × 7	24	25	26	27	28
P_{TX} for N = 8 × 8	22	23	24	25	26
P_{TX} for N = 9 × 9	20	21	22	23	24
P_{TX} for N = 10 × 10	18	19	20	21	22

required, as expected. Considering a square array (N), the data extrapolation from the graphs in Figure 1 can be carried out and it is reported in Table II.

The minimum 70 dBm of EIRP must be guaranteed even when the beam is steered at ±20°. Since a maximum scan loss is expected in the order of 2 dB of steering, the minimum EIRP must be updated to 72 dBm.

In order to have some margin, the combination with EIRP = 74 dBm, with $N = 8 \times 8$ elements and P_{TX} = 26 dBm is chosen for the PAA design. The choice was also motivated considering the achievable average output power P_{TX} of the designed GaN-on-SiC power amplifier (with the hypothesis of 2.5 dB of back-off for a 64-APSK modulation scheme). More details of the amplifier are given in the following section. This preliminary analysis serves to initially size the complexity of the design. The final parameters may change depending on the challenges encountered during the actual design of the amplification stages, as well as the antenna system.

III. GAN-ON-SIC POWER AMPLIFIER

The GaN on SiC power amplifier is designed using UMS foundry's GH15 process, based on AlGaN/GaN epitaxy grown on 4-inch SiC substrate. The transistor features a T gate of 150 nm length, whose shape and fabrication processes have been optimized for ensuring good reliability properties. A source-terminated field-plate is added to reduce the feedback capacitance for a higher gain at RF frequencies. The technology shows a DC saturated drain current around 1.2 A/mm and a DC maximum transconductance (g_m) close to 400 mS/mm.

The substrate is thinned to 70 µm by means of a back-side process that ensures the compatibility with both soldering and gluing-based assembly processes. Other figures of merit of the technology are power density at 30 GHz around 3.5 W/mm and a maximum oscillation frequency (f_{max}) above 80 GHz. These figures demonstrate the technology is well-suited for Ka-band applications. More process details are found in [10] and [11].

The PA design targets, in the 25.5–27.0 GHz band, are 20 dB gain, an output power higher than +25.5 dBm and 30% PAE, to be maximized within the technology limitations.

The first step in PA design is to size the total periphery of the final stage transistor. This step is performed considering the required output power (>25.5 dBm) and considering approximately 1 dB resistive loss of the output matching network (OMN). This leads to approximately 27 dBm at device level (i.e., 500–600 mW). The selected technology can provide a power density of 3.5 W/mm

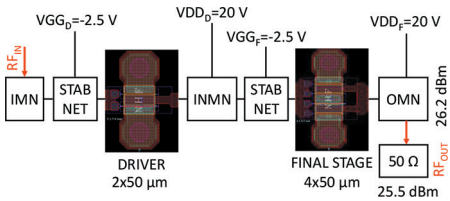

Fig. 2. Simplified PA block diagram.

at +25 V drain voltage. However, we selected to operate the device at a more conservative 3.0 W/mm and +20 V drain voltage to apply space derating conditions, therefore improving reliability. As a result, the total periphery of the final stage is 0.2 mm. A four-finger by 50 µm device is selected to balance the competing requirements of output power, efficiency, and gain. The gain of the final stage is computed to be 10 dB and a two-stage topology is required to achieve a gain greater than 20 dB, sketched in Figure 2.

Another reason for lowering the drain voltage to +20 V is to improve efficiency. Furthermore, the PAE of the single device is approximately 40%; so realistically it is only possible to achieve 30% of PAE in a two-stage PA.

The OMN (Figure 2) is designed to exhibit a purely resistive load at the intrinsic voltage-controlled current source of the final stage transistor. Likewise, to improve efficiency, short circuits are imposed on the higher order harmonics at the same section of the circuit.

The size of the driver (first stage) Field Effect Transistor (FET) is half that of the final stage, as a compromise of linearity, gain, and efficiency at amplifier level. The small-signal gain of active devices is approximately 17 dB while the cumulative loss of passive structures is 3 dB.

Stability networks (STAB NET in Figure 2) are inserted in the HPA to guarantee device unconditional stability over a very wide range of frequencies, practically from 100 MHz to f_{max}.

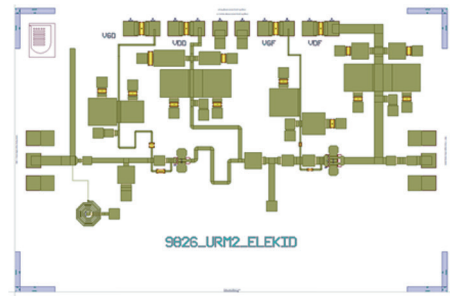

Fig. 3. PA layout. Chip size is 3.0 mm × 2.0 mm.

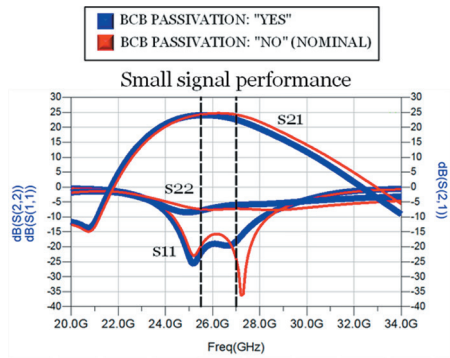

Fig. 4. PA simulated S-parameters. The dashed vertical lines define the operating bandwidth.

Finally, the input matching network and Inter-stage Matching Network (IMN) are designed to provide gain/power terminations at the considered active device's terminals in the operating bandwidth.

The PA's layout is provided in Figure 3. The size is 6 mm^2 and is essentially fixed by the foundry's multi-project wafer run constraints. A smaller chip footprint could have been obtained in a dedicated wafer run. The simulated PA linear performance is shown in Figure 4. The blue traces represent simulations using the benzocyclonbute (BCB) option, while the red traces indicate when the nominal (qualified) manufacturing process is applied. For this manufacturing iteration, we opted for BCB protection, to improve chip ruggedness in harsh operating environments. The DC gate voltage is adjusted around

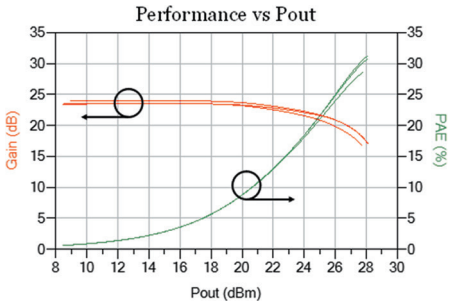

Fig. 5. PA simulated gain and PAE as a function of output power. Three traces are provided for each parameter at 25.5, 26.25, and 27.0 GHz.

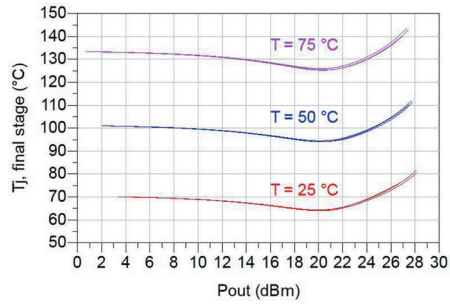

Fig. 6. PA final stage HEMT junction temperature as a function of output power and base-plate temperature 25/50/75 °C. Three traces are provided for each set of data at 25.5, 26.25, and 27.0 GHz.

−2.4 V to obtain an overall DC drain current, in linear operating mode, of 60 mA (20 mA on the driver and 40 mA on the final stage). The DC drain voltage is set at +20 V as per design choice.

The gain is well above 20 dB in the range of 25.5–27.0 GHz. As shown in Figure 4, and the input matching is better than 15 dB, while the output matching is between 7 and 10 dB depending on the selected production process.

The PA's simulated nonlinear performance is provided in Figure 5. The saturated output power reaches +28 dBm, therefore fulfilling the >25.5 dBm requirement. For this high output power level, the PAE reaches 30% while requiring more than +10 dBm input power. If the PA is operated in back-off, around +25.5 dBm output power, then the PAE is reduced to 23%. The advantage is that a significantly lower RF input power is required, which is only +5 dBm. The overall DC drain current reaches 80 mA at +26 dBm output power and 100 mA at saturated output power (+28 dBm).

Lastly, the final stage HEMT junction temperature (T_j) is plotted in Figure 6. This parameter is critical to ensure adequate device reliability. Recent indications by the European Space Agency (ESA) reported in [12] recommend this value should remain below +160 °C to ensure adequate reliability in components employed in spaceborne payloads. This channel temperature operation is obtained by design, applying the synthesis methodology reported in [13] where the classical power amplifier design paradigm is reconsidered shifting to a thermal-aware design approach. The MMIC has completed the manufacturing process and is currently being tested to verify the compliance with design targets and simulated data.

IV. ESKAA SYSTEM ARCHITECTURE

The proposed concept is envisaged as a 64-element transmitting only PAA operating in the lower portion of the Ka-band. Table I summarizes the most important features of the intended antenna system, but this section deals with the foreseen architecture of the overall printed circuit board (PCB) and antenna assemblies, sketched as a simplified block diagram in Figure 7.

The phased array is based on a complex electronic system designed onto a 12-metal layer 200 mm × 200 mm PCB. The copper clads and layers are mixed per type and thickness to accomplish different tasks. The top layer is

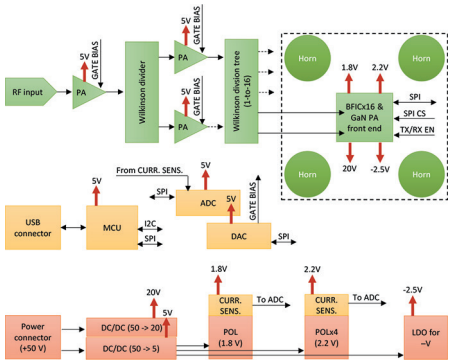

Fig. 7. System block diagram of the phased array. RF paths (green), digital and monitoring functionalities (yellow), and power tree (red) have been highlighted in this sketch.

principally devoted to route the Ka-band signal. A 4-mil Rogers 4350B LoPro has been chosen as premium RF material with a 17 µm copper foil featuring a very low surface roughness. Down to the fifth copper layer, the chosen dielectrics are larger in thickness but very similar to the top one per electrical proprieties. This choice guarantees optimal performance in the microstrip-to-waveguide launcher, exploited as feeding system for each horn antenna. From fifth to the bottom layer, the dielectrics are FR4-like since no RF signal is routed. The copper clads of inner layers have been chosen accordingly to their main functionalities: layers 3 and 6 are 35 µm thick to route the +5 V supply up to 20 A, layers 9 and 11 are 70 µm thick to supply the beamformer ICs with the +1.8 V and +2.2 V high-current rails, and the remaining layers are 17 µm thick to mainly support digital signals and medium-to-low power supplies.

The RF architecture relies on single feeding point, designed as a 2.92 mm end-launch connector. Then, a planar splitter tree based on a cascade of custom-designed Wilkinson divider and the series of two gain block feeds with 16 ICs. Each chip has two common input ports and is foreseen to be connected to the final PA stage and serves a sub-array of 2 × 2 horns. The overall network embeds 31 splitters loaded with 0201 commercial 100 Ohm resistors, rated up to 50 GHz. Given the top-layer physical and electrical features, the calculated loss per unit length of the 50 Ohm microstrip has been computed as 24 dB/m with an overall routing of 200 mm. The analog front-end finally exploits the GaN-based PA, described in the previous section, which directly feeds the antenna through ad-hoc launchers.

The PAA design also includes digital features. A microcontroller unit (MCU) is exploited to manage Serial Peripheral Interface (SPI) connection with the beamformer ICs. Digitally controlled multi-channel digital-to-analog convertors are also embedded to finely adjust the analog PA gate biasing and to partition each drain supply for a programmable start-up sequence. Analog-to-digital convertors are used to read current sensors placed along the main supply rails. Standard USB connectors enable the MCU programming through an external device.

A single power supply of +50 V is chosen to fully bias the system. A three-polar connector is mounted directly onto the PCB and connected to the main DC/DC isolated power converters through a capacitor filtering scheme, a fuse in case of short circuit, and a circuit to prevent reverse polarization biasing. The down-conversion drops the supply to +5 and to +20 V. The main +5 V rail is then routed to five non-isolated DC/DC point of load converters. One is devoted to down-convert the +5 to +1.8 V up to 12 A, whereas the other four convert the main rail to +2.2 V up to 8 A each. The main supplies +5 and +20 V directly bias the drains of the RF gain blocks and the final PA stages, respectively. An Low-Dropout regulator

(LDO) is also present to generate the negative supply voltage of −2.5 V, needed for the gate biasing of the power amplifiers.

The arrangement of the components on the circuit board needs to be properly taken into account. The split of PCB layout into different functional areas (RF, digital, and power) is one golden rule in electronic design, especially in a complex system like a PAA. Additionally, the overall assembly needs to accommodate also waveguide structures to feed the matrix of 64 circular horn antennas.

Each microstrip-to-circular waveguide launcher is designed on the top layer of the PCB where the lowest RF losses are expected and where the whole RF circuit is foreseen. However, the launcher needs a circular backshort; then the stack-up thickness has been designed to match exactly the quarter-wavelength dimension needed by the transition. To diminish the losses, lower FR4-like layers are milled in correspondence of each waveguide feed. Contrarily, the upper low-loss dielectric layers fully cover the circular section allowing the penetration of the microstrip launchers inside the waveguide footprint and reinforce the membrane beneath the antenna structure.

The whole PCB is supported by a flat metallic carrier, made by aluminum. A silver finishing is foreseen since each waveguide backshort is sealed by the metallic surface. The carrier is then machined to allow a perfect matching with the components placed on the bottom side of the stack-up. The overall assembly is then closed by a cover, fully machined from a single aluminum block. The cover has multiple functions: it acts as antenna since all the 64 circular horns are engraved into this top part, but it also serves as heatsink for the beamformer ICs and the main DC/DC converter. The overall weight of the bottom and top mechanical parts is in the order of 1.2 kg.

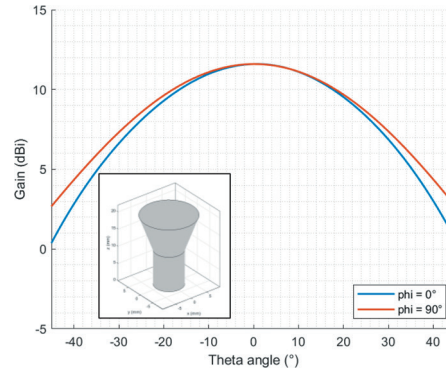

Fig. 8. Directivity cuts for Φ = 0°/90° and 3D view of the basic radiating element.

V. UNIFORM GRID ANTENNA SIMULATIONS

The first implementation of ESKaA is envisioned as a uniform grid of 8 × 8 circular horns.

The design of the basic antenna has been addressed considering the trade-off in the phased array design. A larger antenna element will result in a larger pitch between each radiator than a higher gain but lower steering capabilities. On the contrary, a matrix of smaller horns can address wider steering angles at the cost of an overall lower array factor gain. The balance has been found considering the regular lattice of 64 horns delivering 12.2 dBi of gain.

The preliminary antenna design follows general rules of circular horn synthesis, well described in [14]. The input waveguide is 8 mm in diameter, whereas the aperture diameter is 15.2 mm. The horn's flare is set as 10 mm, an optimal trade-off between aperture efficiency, input matching and thickness of the foreseen metallic cover, which has to accommodate the antennas. Figure 8 shows the directivity of the basic element estimated through an antenna synthesis. The slight differences in the Half Power Beamwidth (HPBW) between the 0° and 90° cuts are aligned

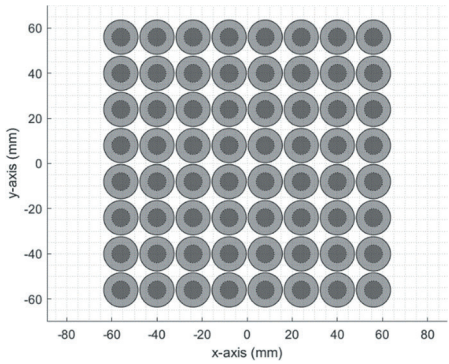

Fig. 9. Lattice of 64-horn antenna elements. Dark gray dotted circles show the footprints of the input circular waveguides, whereas the larger gray circles mimic the 15.2 mm horn apertures.

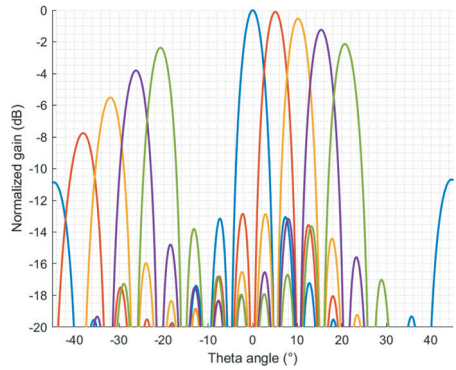

Fig. 10. Array directivity versus theta angle for $\Phi = 0°$ in different steering configurations, from boresight direction to 20° tilt.

with the fact that the formulas refer to a linear polarized feeding. A preliminary 3D view of the antenna is also shown in Figure 8 to highlight the involved aspect ratio between input waveguide diameter, the horn's aperture, and the flare length.

The array is the composition of the basic radiators in a uniform square lattice of 8 × 8 elements, as sketched in Figure 9. The normalized radiation pattern of the array is shown in Figure 10. The maximum gain is however lower with respect to the target since it stops to 26.9 dBi. The overall EIRP of the system is then 71 dBm when combined with the total output power of 26 dBm from the 64 antennas. The graphs in Figure 10 also show the theoretical beamsteering performance of the PAA. The evaluated tilted angle is up to 20°, which is the maximum allowed to be free from grating lobes in the observation range of ±20°. Thanks to the normalization, the scan loss is highlighted and evaluated in 0.11 dB/°. First secondary lobes appear to be −13 dB from the peak gain, without applying any amplitude tapering.

The center-to-center distance of 16 mm, equal to $0.71 \cdot \lambda_0$ calculated at 26.25 GHz, makes the square footprint of the array of 128 mm^2. The compactness of the array perfectly fits the designed square PCB of 200 mm^2. The remaining areas surrounding the antenna-only footprint are devoted to accommodate the power supply elements and the digital architecture.

Preliminary antenna synthesis did not take into account any full-wave simulations. However, the foreseen real implementation of the horn antenna array will be based on CNC machining to guarantee extremely tight accuracy and smooth surface finishing. The horn's flare will be approximated with a 1 mm stepped profile in place of an ideal smooth one. This method allows to significantly reduce the manufacturing complexity and speed up the machining time. Silver plating is also foreseen on top of aluminum to lower ohmic losses involved in the waveguide feeding system and into each hollow antenna.

VI. CONCLUSION

This paper introduces the ESKaA concept, a transmitting only PAA for Ka-band applications. The manuscript gives details in terms of system sizing, envisaged PCBA architecture, and overall performance. Core of the PAA is the GaN PA, specifically designed to match the

requirements in terms of output power and PAE, expected to be as high as 28 dBm and 30%, respectively. Simulations of the 64-element antenna array show a maximum boresight gain of 26.9 dB and an addressable steering angle up to 20°.

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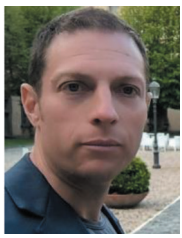
Rocco Giofrè (Senior Member, IEEE) received the Ph.D. degree in electronics from the University of Rome Tor Vergata, Rome, Italy, in 2008. He joined the Electronics Engineering Department, University of Rome Tor Vergata, in 2009, where he is currently an associate professor of electronics. He has authored more than 200 peer-reviewed articles, two book chapters, and two contributions for the Wiley Encyclopedia of Electrical and Electronics Engineering. His research activities belong to the microwave and millimeter-wave electronics area ranging from active device characterization to the design and test of linear and nonlinear circuits and systems. In this wide research area, he is mainly focused on the development of innovative power amplifier schemes and architectures with high efficiency and linearity for both ground and space communication systems, including their integration in multifunctional chips such as single-chip front-ends. He is involved in many research projects funded by international research agencies, such as the European Space Agency (ESA) and the Research Executive Agency (REA), European Commission, Brussels, Belgium. Dr. Giofrè is a member of the IEEE MTT-S Subcommittee 12 on power amplifiers, an associate editor for IEEE Access Journal, and a reviewer for the major journals and conferences of the field. He was a recipient of the 2005 Young Graduated Research Fellowship presented by the GAAS Association and the Best Paper Award at the EuMIC 2007.

Ernesto Limiti (Senior Member, IEEE) was a research and teaching assistant (1991–1997), an associate professor (1998–2001), and since then has been a full professor of electronics with the EE Department, University of Roma Tor Vergata, Rome, Italy. He has authored or co-authored over 500 publications on refereed international journals and presentations within proceedings of international conferences. His research activity is focused on three main lines, all of them belonging to the microwave and millimeter-wave electronics area. The first one is related to characterization and modeling for active and passive microwave and millimeter-wave devices. Regarding active devices, the research line is oriented to small-signal, noise, and large-signal modeling. For active devices, novel methodologies are developed for the noise characterization and the subsequent modeling, and equivalent-circuit modeling strategies are implemented both for small- and large-signal operating regimes for GaAs, GaN, SiC, Si, and InP MESFET/HEMT devices. The second line is related to design methodologies and characterization methods for low-noise devices and circuits. The main focus is on cryogenic amplifiers and devices. Finally, the third line is in the analysis and design methodologies for linear and nonlinear microwave circuits. Prof. Limiti is a referee for international journals of the microwave and millimeter-wave electronics sector. He is a member of

the Steering Committee of international conferences and workshops. He has been the president of the Laurea and Laurea Magistrale degrees in electronic engineering of the University of Roma Tor Vergata, and is a member of the committee of the Ph.D. program in telecommunications and microelectronics, tutoring an average of four doctoral candidates per year. He is currently the Head of Electronic Engineering Department and the director of the Microwave Engineering Center for Space Applications (MECSA).



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