Sub-THz Transceiver Design for Future Generation Mobile Communications

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Abstract—**This paper outlines the design considerations necessary to realize an innovative transceiver prototype for future-generation mobile communication, adeptly harnessing the spectrum beyond 100 GHz. The primary innovations and challenges reside in maximizing the efficacy of BiCMOS and indium phosphide technologies, advanced radio frequency (RF) packaging, and the design of high-performance D-band RF front-ends. The selection of RF-chip technologies and the integration of densely packed RF packaging are thoroughly defined and justified. Specifications for both transmitter and receiver systems are derived from a meticulous link budget analysis. These preliminary studies and decisions inform the forthcoming tape-outs in this project. The focus remains on developing key transceiver technologies to drive the next generation of mobile communications, surpassing the capabilities of 5G. This includes enhancing data rates, power efficiency, integration density, and minimizing footprint.**

Index Terms—**6G mobile communication, antenna-in-package, BiMOS integrated circuits, InP, integrated circuit packaging, millimeter wave integrated, mobile communication, phased arrays, receivers, transmitters**

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I. INTRODUCTION

ACCORDING to market analysts, the proliferation of smart devices is expected to continue, contingent upon technological advancements. Devices like augmented reality glasses require high bandwidth connectivity, efficient operation, and dense integration. Utilizing higher frequency bands above 100 GHz holds significant potential to meet these emerging system requirements and also presents severe technical challenges. Within the SHIFT (Sustainable

technologies enabling Future Telecom applications) project, a Chips JU initiative focused on advancing sustainable technologies to enable future telecom applications, we are developing a "Future-G transceiver" prototype. This prototype leverages the D-band radio spectrum to achieve the demanding requirements of speed and bandwidth.

Currently, such operating frequencies are restricted to wireline communication, while long-range wireless links beyond 100 GHz are only established for static applications (i.e. back/front-hauling) rather than for mobile applications. At these frequencies, hardware validation necessitates most advanced measurement and lab infrastructure. Most developed demonstrators are still using horn antennas, which are neither integrated nor compact.

In addition to high frequency, technology must also support efficiency. Recent advancements in BiCMOS systems, for instance, demonstrate data rates of tens of Gb/s in the frequency bands above 100 GHz [1][2][3]. However, the limited output power of this technology restricts the link distance to a few centimeters. Conversely, III-V technologies, such as indium phosphide (InP) from III-V Lab, allow for efficient and high radio frequency (RF) performance beyond 100 GHz [4][5].

We address efficiency by combining (i) ST BiCMOS B55X technology [6], known for its state-of-the-art performance in RF and mixed signal on silicon, with (ii) III-V-Lab's InP technology, which provides superior amplification efficiency and power delivery beyond 100 GHz. A system study illustrating the benefits of combining silicon transmitters (TXs) with InP power amplifiers (PA) is shown in Figure 1 [7]. This study demonstrates that for an N-path phased-array TX with a total equivalent isotropic radiated power (EIRP) of 40 dBm, the combination of a silicon-based system with InP

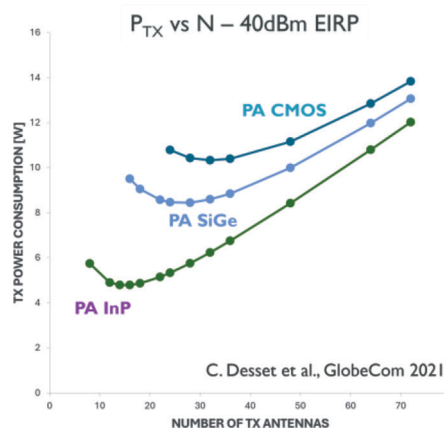

Fig. 1. Study in [7]: benefit of combining InP PAs with Silicon-based phased-array sub-THz transmitter.

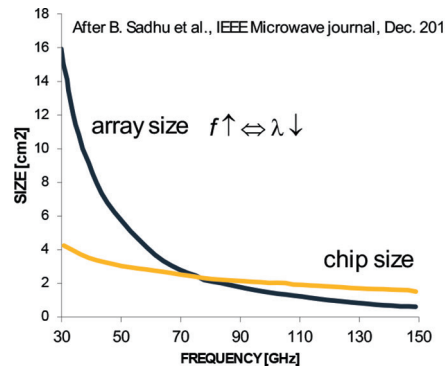

Fig. 2. Array size versus chip size, after [8].

PAs reduces both power consumption and the optimal number (N) of antennas.

Beyond high operating frequency and efficiency, RF packaging poses significant challenges in terms of signal losses and size. At frequencies beyond 100 GHz, antenna gain decreases while the connectivity loss between on-chip amplifiers and antennas increases. Moreover, the size of the phased-array becomes comparable to the chip size, as shown in Figure 2, after the study in [8].

Our work addresses key innovations and challenges in developing integrated solutions for future high-speed mobile communication. These include

TABLE 1.
SCENARIO KEY PERFORMANCE INDICATORS.

Demonstrator KPI	Scenario‘s targets	Demonstrator‘s targets
Data rate	2 channels – 60 Gsps	1 channels – 30 Gsps
Bandwidth	2 × 5GHz in dual polarization	5 GHz in single polarization
Range	100 m	5m
Tx EIRP	24dBm	24dBm
Form factor	12 antennas	4 antennas
Frequency of operation	~140 GHz	~140 GHz
Modulation order	64 QAM	16 QAM
Transmit power and efficiency	18 dBm OCP1 dB 20% PAE max	16 dBm OCP1dB 10% PAE max

the optimal selection and utilization of chip technologies such as BiCMOS and InP, the design of high-performance and efficient D-band (140 GHz, wideband) TX and receiver (RX) front-ends, and advanced RF packaging. Starting with a high-data-rate link budget scenario in Section II, initial specifications for the TX and RX front-ends are derived in Section III. Various aspects of the implementation are detailed in Section IV, and conclusions are presented in Section V.

II. SCENARIO OF HIGH DATA-RATE LINK

The scenario considered in this demonstrator involves establishing a high-data-rate communication link between a base station (BS) and user equipment (UE) in environments such as airports or shopping malls. Table I outlines the key performance indicators (KPIs) for the proposed scenario. Note that while the system is designed to meet the scenario’s targets, the requirements have been moderated for the final demonstrator. This approach is intentionally adopted to mitigate risks and ensure a functional demonstrator within the project SHIFT’s timeframe.

The link budget assumes a line-of-sight (LoS) link between a BS and a mobile UE, aiming to cover distances up to 100 m. The system aims to achieve a raw data rate of up to 60 Gbit/s with dual polarization and 30 Gbit/s with single polarization (maximized in downstream, can be smaller in upstream). Given a single stream of 30 Gbit/s and a raw spectral efficiency of 6 bit/s/Hz using 64 quadrature-amplitude modulation (QAM), the required channel bandwidth is 5 GHz.

The EIRP and the total radiated power (TRP), crucial specifications for the link budget, are drawn from the ETSI 5G FR2 standard [9]. That because D-band communication is not yet standardized. In our scenario, the baseband TX is referred to the power class 1, imposing limits of 55 dBm for EIRP and 35 dBm for TRP. Conversely, the handheld UE TX falls under power class 3, with EIRP and TRP limited to 43 and 23 dBm, respectively.

The link budgets for the downstream reception at the user equipment (UE RX) and upstream transmission from the user equipment (UE TX) are illustrated in Figures 3 and 4. In these figures, we utilize the modulation-and-coding scheme (MCS) of the WiGiG 60-GHz standard [10] chosen for its ability to accommodate a much wider bandwidth compared to current 5G FR2 standards. The TX output 1-dB compression point (OP1dB) is deliberately specified, and the number of antennas on the TX and RX sides is carefully adjusted

MCS (derived from WiGig)	0	9	13	17	
Constellation	D-BPSK	QPSK	16QAM	64QAM	
LDPC code rate	1/2	13/16	13/16	13/16	
Spreading/repetition	32	1	1	1	
raw data rate	5000	10000	20000	30000	Mbps
Frequency					
Carrier frequency	140000				MHz
wavelength (lambda)	0.0021				m
bandwidth	5000				MHz
roll-off	0				
TX (basestation)					
Tx power per PA (output P_1dB)	12.00	14.00	16.00	18.00	dBm
Number of antennas per sub-array (TX)	1.00	1.00	1.00	1.00	
Number of sub-arrays (TX)	128.00	128.00	128.00	128.00	
Lens gain	0.00	0.00	0.00	0.00	dB
Antenna element gain	5.00	5.00	5.00	5.00	dBi
Total array gain (20log(Ntx) + ...)	47.14	47.14	47.14	47.14	dB
TX interconnect loss (<0 dB)	-4.00	-4.00	-4.00	-4.00	dB
Back-off from P_1dB (>= 0)	0.00	2.00	4.00	6.00	dB
Total EIRP	55.14	55.14	55.14	55.14	dBm
TRP	29.07	29.07	29.07	29.07	dBm
Channel					
LOS loss	-141.35	-121.71	-114.79	-105.88	dB
Atmospheric attenuation factor (LOS)	**0.000**				dB/m
Atmospheric attenuation (with range)	0.00	0.00	0.00	0.00	dB
RX (UE)					
Number of antennas per sub-arrays (RX)	1.00	1.00	1.00	1.00	
Number of sub-arrays (RX)	12.00	12.00	12.00	12.00	
Lens gain	0.00	0.00	0.00	0.00	dB
Antenna element gain	5.00	5.00	5.00	5.00	dBi
Total array gain (10log(Nrx) + ...)	15.79	15.79	15.79	15.79	dB
RX interconnect loss (<0dB)	-4.00	-4.00	-4.00	-4.00	
Received power including array gain	-74.42	-54.78	-47.85	-38.94	dBm
Thermal noise	-77.01	-77.01	-77.01	-77.01	dBm
Noise figure	9.00	9.00	9.00	9.00	dB
Implementation loss (Analog and Digital)	-3.00	-3.00	-3.00	-3.00	dB
EVM from non-additive effects (phase noise, ...)	-23.00	-23.00	-23.00	-23.00	dB
Link margin	2	2	2	2	dB
Input referred noise (including EVM)	-63.01	-62.87	-62.35	-59.43	dBm
SNR, Range, Bit rate					
Required SNR (coded BER = 3e-7)	-11.40	8.10	0.00	0.00	dB
Achieved SNR	-11.41	8.09	14.50	20.49	dB
SNR difference - link margin	-0.01	-0.01	14.50	20.49	dB
Max range	1992.73	207.71	93.59	33.55	m

Fig. 3. Link budget for UE RX downstream.

MCS (derived from WiGig)	0	9	13	17	
Constellation	D-BPSK	QPSK	16QAM	64QAM	
LDPC code rate	1/2	13/16	13/16	13/16	
Spreading/repetition	32	1	1	1	
raw data rate	5000	10000	20000	30000	Mbps
Frequency					
Carrier frequency	140000				MHz
wavelength (lambda)	0.0021				m
bandwidth	5000				MHz
roll-off	0				
TX (UE)					
Tx power per PA (output P_1dB)	14.00	16.00	18.00	18.00	dBm
Number of antennas per sub-array (TX)	1.00	1.00	1.00	1.00	
Number of sub-arrays (TX)	16.00	16.00	16.00	16.00	
Lens gain	0.00	0.00	0.00	0.00	dB
Antenna element gain	5.00	5.00	5.00	5.00	dBi
Total array gain (20log(Ntx) + ...)	29.08	29.08	29.08	29.08	dB
TX interconnect loss (<0 dB)	-4.00	-4.00	-4.00	-4.00	dB
Back-off from P_1dB (>= 0)	0.00	2.00	4.00	6.00	dB
Total EIRP	39.08	39.08	39.08	37.08	dBm
TRP	22.04	22.04	22.04	20.04	dBm
Channel					
LOS loss (Friis)	-135.57	-115.93	-109.01	-98.10	dB
Atmospheric attenuation factor (LOS)	**0.000**				dB/m
Atmospheric attenuation (with range)	0.00	0.00	0.00	0.00	dB
RX (basestation)					
Number of antennas per sub-arrays (RX)	1.00	1.00	1.00	1.00	
Number of sub-arrays (RX)	128.00	128.00	128.00	128.00	
Lens gain	0.00	0.00	0.00	0.00	dB
Antenna element gain	5.00	5.00	5.00	5.00	dBi
Total array gain (10log(Nrx) + ...)	26.07	26.07	26.07	26.07	dB
RX interconnect loss (<0dB)	-4.00	-4.00	-4.00	-4.00	
Received power including array gain	-74.42	-54.78	-47.85	-38.94	dBm
Thermal noise	-77.01	-77.01	-77.01	-77.01	dBm
Noise figure	9.00	9.00	9.00	9.00	dB
Implementation loss (Analog and Digital)	-3.00	-3.00	-3.00	-3.00	dB
EVM from non-additive effects (phase noise, ...)	-23.00	-23.00	-23.00	-23.00	dB
Link margin	2	2	2	2	dB
Input referred noise (including EVM)	-63.01	-62.87	-62.35	-59.43	dBm
SNR, Range, Bit rate					
Required SNR (coded BER = 3e-7)	0.00	0.00	0.00	0.00	dB
Achieved SNR	-11.41	8.09	14.50	20.49	dB
SNR difference - link margin	-11.41	8.09	14.50	20.49	dB
Max range	1024.03	106.74	48.10	13.70	m

Fig. 4. Link budget for UE TX upstream.

to achieve a 100-m link distance without exceeding the EIRP or TRP limits. For the UE RX downstream, a distance of 100 m is only achievable for modulation schemes

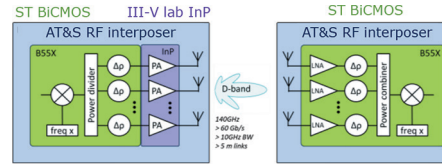

Fig. 5. Transmitter front-end integrating BiCMOS and InP chips within an advanced RF packaging (on the left) and receiver front-end integrating a BiCMOS chip within an advanced RF packaging (on the right).

up to 16 QAM, with a raw data rate up to 20 Gb/s, but not for 64 QAM, which offers a raw data rate of 30 Gb/s. Similarly, for the UE TX upstream, a distance of 100 m is only feasible for modulation schemes up to QPSK (Quadrature Phase Shift Keying), providing a raw data rate up to 10 Gb/s. It is important to note that these specifications are intended for the system (and subcircuits) design purposes, and the requirements for the final demonstrator will be relaxed to mitigate risks.

III. SPECIFICATIONS

The integration concept of TX and RX envisioned in this project is shown in Figure 5. The RX front-end has a chip in ST BiCMOS B55X technology, embedded within an advanced RF packaging by AT&S [11]. The TX front-end comprises a chip in B55X and last stages of PAs in III-V-Lab InP technology. To showcase beamforming, both TX and RX implement phase-shifting array on chip.

Two 5-GHz channel bandwidths are targeted: from 143.5 to 148.5 GHz and from 151.5 to 156.5 GHz. These are a part of the four bandwidths recommended by [12], as shown in Figure 6. Accordingly, the TX and the RX front-ends are specified to work from 143.5 to 156.5 GHz.

A. *Transmitter*

The primary specifications for the transmitter (TX) front-end, as determined from

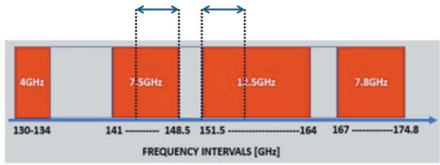

Fig. 6. Channel bandwidths recommended by [12], and targets for this project: 143.5–148.5 GHz and 151.5–156.5 GHz.

the link budget (Figure 4), include output power, bandwidth, and signal-to-noise ratio (SNR). Additionally, a key focus is placed on achieving the overall efficiency. The output power is currently set at a 1-dB compression point of 18 dBm. However, ongoing studies are exploring the trade-off between this high power requirement and the efficiency of InP, which may result in a potential downgrade of this specification to 15 dBm. Ensuring an SNR well above 23 dB for a coded 64-QAM modulation scheme is crucial. To achieve this, we have opted for an up-conversion transmitter (TX) topology based on a wideband intermediate frequency (IF) instead of a zero-IF one. This decision helps mitigate SNR degradation caused by baseband direct current (DC) offset and in-phase/quadrature (I/Q) imbalance.

B. Receiver

We propose a four-path RX architecture, shown in Figure 7, as a trade-off between ease of integration in phased arrays, silicon area, power consumption, and heat dissipation. The considered application requires four RX antenna paths, synchronized by their common frequency reference input. The noise figure of the RX is reduced by the shrinking of the antenna interconnection length due to 3D packaging, and innovative LO phase shifting, instead of lossy RF phase shifting (vector modulator, switched delay cells, etc.). We expect to save power consumption and area while improving

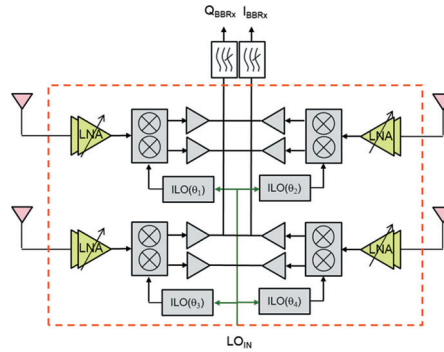

Fig. 7. Proposed receiver architecture.

TABLE II.
MAIN RECEIVER SPECIFICATIONS.

Receiver	Gain: 10–57 dB, NF: 9 dB, BW: 142.5–157.5 GHz
LNA	Gain: 18/10 dB, NF: 7.5 dB, IIP3: −15/−7 dBm
I/Q mixer	Gain: 3/−9 dB, NF: 20 dB, IIP3: 3/11 dBm, 3° phase imbalance
LOin	Frequency: 36.5/38.5 GHz, Phase noise: −107 dBc/Hz@1 MHz & −137dBc/Hz noise floor
Phase shifters	2 + 4 bits resolution

performance. Here we consider zero-IF direct conversion mixing over a wide bandwidth (2 × 2.5 GHz).

From the lowest sensitivity level to the maximum input power, the RX shall cope with a power dynamic range of 47 dB, from −67 to −20 dBm. Part of it (30 dB) shall be handled by the base band variable gain amplifier (VGA). Moreover, low gain modes shall be considered for low-noise amplifier (LNA) and mixer to de-saturate the RX. A summary of specifications is shown in Table II.

IV. IMPLEMENTATION

A. Transmitter Front-End in BiCMOS

The TX architecture proposed in the SHIFT project, shown in Figure 5,

incorporates a wideband IF system, followed by a BiCMOS phased-array TX front-end, used to drive InP PAs. An RF interposer will be used to host the BiCMOS/InP chips and to integrate antennas and interconnections.

In the BiCMOS TX front-end, the IF signal is up-converted to the D-band frequencies using a mixer. The local-oscillator (LO) signal is generated at a lower frequency and then a frequency multiplier is used to drive the mixer LO port. To avoid the severe losses of passive mixers, the TX up-conversion mixer topology is Gilbert cell-based. The output 1-dB compression point of the Gilbert cell block must be carefully designed to make sure that the mixer does not introduce severe compression to the chain under the large input power level required to saturate the PAs. A wideband matching at the IF port is achieved by either using a resistive-feedback inverter or by adding a resistive termination at the gate of the IF transistors to reduce the input impedance. The LO power level required to achieve acceptable linearity and gain is determined so that saturated LO drivers deliver this power level to the LO transistors with reasonable efficiency.

Following the mixer, power dividers are used to drive the phase shifters. For power splitters, the Wilkinson topology offers scalable power splitting with good isolation between the array elements. Wilkinson power splitters can be implemented based on transmission lines, lumped components, or transformers. Although transmission-line-based Wilkinson dividers generally have low loss, wide bandwidth, and are simple to implement, they are usually not adopted on chip at lower RF/mmWave frequencies (e.g., 30 GHz) due to the large area they require ($\lambda/4 \sim 2.5$ mm at 30 GHz). However, at 150 GHz, $\lambda/4$ drops to 500 μm or even lower length; therefore, transmission-line-based Wilkinson power splitters can be feasible at D-band with reasonable area. With such a transmission-line-based Wilkinson topology, matching and isolation > 12 dB can be expected and an insertion loss of around 0.5 dB (on top of the 3 dB fundamental loss) is expected across the whole D-band.

Finally, phase shifters precede the InP PAs. Phase shifters typically build active vector modulators or passive implementations. The latter mainly include reflective-type phase shifters, switched-type phase shifters, or switchable transmission lines. Reflective-type phase shifters require high-order loads (e.g., *CLC* loads) and/or cascading multiple units to achieve the 360° phase range. However, in the D-band, on-chip varactors often exhibit significant losses and offer limited capacitance tuning range. As a result, these limitations can lead to increased insertion loss or a reduction in the achievable phase range. Similarly, utilizing switched-type phase shifters or switchable transmission lines may necessitate a cascade of multiple stages with numerous switches, thereby increasing the insertion loss of the phase shifter to over 10 dB at D-band. To circumvent the insertion loss associated with passive implementations, the transmitter (TX) phase shifters will be based on a vector modulator architecture. VGAs using multiple cells of common-source stages should be implemented with different gain weights, connected in parallel. The power combination of the I/Q components by summing the outputs of the VGAs in the current domain, and the 0°/180° phase flipping is achieved by switching the terminals of the differential output. The phase shifters are planned with 4-bit accuracy (22.5° phase resolution) accordingly. Such a BiCMOS

front-end will drive high-power InP PAs on the same interposer.

B. Power Amplifiers in InP

The InP DHBT (Double Heterojunction Bipolar Transistor) technology of III-V Lab [4] is natively optimized for high-speed analogue–digital electro-optical interfaces (for optical fiber applications): transistor's figures of merit are optimized for fast current switching, high voltage drive, and wideband operation. The first run of D-band PA in SHIFT is therefore essentially an evaluation of the achievable performance with respect to the state-of-the art, which will serve as a guideline for (i) improving transistor design and (ii) selecting circuit design options and techniques (power cell topology, matching methods, power combining options, etc.). The used 0.5-µm InP DHBT technology has an fT/fMAX ~ 380/520 GHz for a 0.5 × 5-µm2 device at Vce = 1.6V and Jc = 7 mA/µm2. Besides fT and fMAX, the breakdown voltage (BVceo = 4.2 V) and knee-voltage (Vk ~ 0.8 V) are also important metrics for PAs that are directly impacting output power (P_{sat}) and power-added efficiency (PAE). To estimate realistic expectations, an idealized parallel-tuned prototype PA has been initially considered, which showed an advantage for the class-AB operation in terms of PAE and P_{1dB} (compression point). Based on this, the common-base PA topology is shown in Figure 8.

The layout is based on thin-film microstrip lines for compactness and overall lowest interconnect loss. The design exploits two-finger 0.5 × 5-µm2 devices for the power stage and single-finger 0.5 × 7-µm2 device for the driver. The chosen topology draws inspiration from [5].

Initial simulation results indicate a gain G_{ss} = 8.5 dB, P_{1dB} = 12.2 dBm and PAE_{max} = 13.4% at 140 GHz. These findings

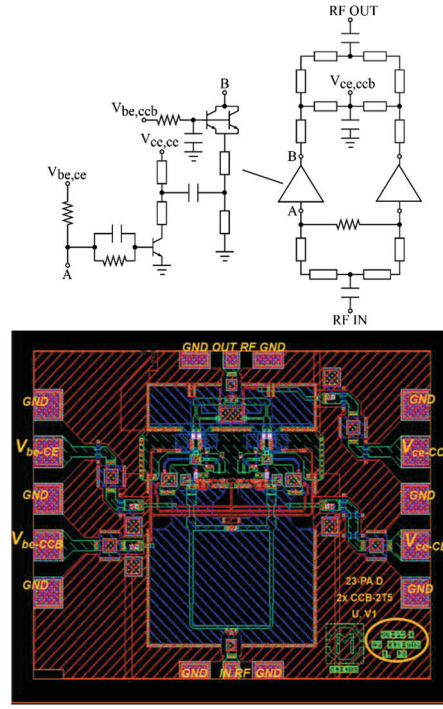

Fig. 8. Simplified schematic and layout of two-way combined power amplifier using common-base power stage with base capacitance and common-emitter driver.

underscore the necessity of employing 0.4 µm emitter width devices and optimized multi-finger DHBTs to enhance performance further. Currently, this endeavor is underway in preparation for the upcoming fabrication run. As anticipated, this initial design serves as a valuable reference point for future enhancements and aids in the selection of viable technology optimization strategies.

C. Wideband Intermediate Frequency

Generating a 5-GHz bandwidth signal at 150 GHz introduces a major challenge in designing both the baseband and the RF sections of the TX in a direct up-conversion architecture, especially

if the error-vector-magnitude (EVM) layer must meet 64-QAM modulation requirements.

A preferable choice is to create a wideband IF signal, based on a multi-carrier approach, which alleviates baseband complexity and ensures accurate LO quadrature generation with moderate power consumption.

The TX is tested with a 5-GHz bandwidth signal having IF placed between 4 and 5 GHz, which combines 4–8 channels together, each with maximum bandwidth of 100 MHz, EVM and quadrature accuracy commensurate with 64QAM modulation.

This solution adds flexibility for signal allocation within the bandwidth: in a non-contiguous scenario, the 4–8 channels can be distributed between 2 and 7 GHz, while in a contiguous scenario, the 400- to 800-MHz bandwidth supports multi-carrier performance evaluation.

D. Receiver Front-End in BiCMOS

In this paragraph, we will provide a brief overview of the implementation of the key blocks of the RX. The first critical building block is the LNA, with its most challenging specification being the noise figure. The schematic selected for the LNA is depicted in Figure 9. It features a classical two-stage cascode topology with input, inter-stage, and output matching networks based on transmission lines. Due to the limited maximum gain of bipolar transistors at 150 GHz, the LNA requires two cascode stages to achieve the specified overall gain.

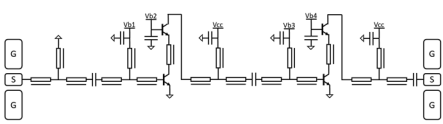

Fig. 9. LNA schematic.

The matching network topology ensures DC biasing through parallel stubs, and DC isolation between stages using link capacitors. Stubs are alternating current (AC) short-ended using custom decoupling capacitors. Matching networks are EM-simulated including capacitors to obtain reliable results.

Our first analysis of the topology shows that we can reach more than 20 dB of gain in the targeted bandwidth with a noise factor of 6.5 dB, leaving some room for the interconnection losses. Further investigations are ongoing to improve even more performance.

To generate the four quadrature phase-shifted LOs, we utilize the architecture depicted in Figure 10. Every path is fed by the same frequency reference that operates at one-fourth of the carrier frequency (36.5 and 38.5 GHz). The signal is multiplied by 2 in frequency, before rough phase shifting on 2 bits (0/45/90/135°) at 73 or 77 GHz. The signal is then again multiplied by 2 before the fine phase shifting, operated at the carrier frequency by an injection-locked phase shifter (ILPS). From Adler's theory [13], the output injection-locked-oscillator (ILO) phase shift varies between +/–90° within the locking range. We propose to use

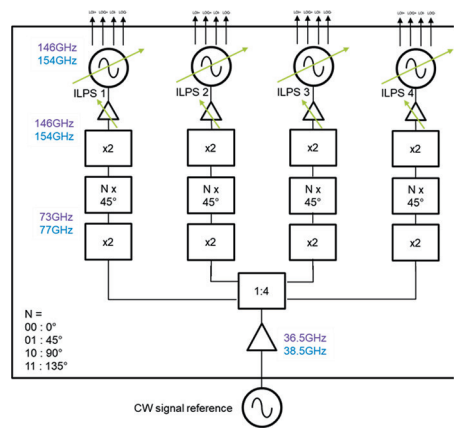

Fig. 10. Multi-LO frequency synthesis architecture.

only part of this range (+/–45°) for fine phase shifting, in order to guarantee locking margin and linear behavior close to zero. The phase shift can be obtained by playing on its natural pulsation through the variation of the ILO tank capacitance (switched capacitance and/or varactor tuning). It is also possible to adjust phase shift and locking range though the variation of the injection level [14]. The phase shifts to apply on the LOs are coded over 2 + 4 bits: 2 bits for the rough phase shifter, and 4 bits for the fine ILPS phase shifter. A 5-bit quantization is enough to generate beams with 3° angle steps and 0.25-dB inter-beam loss. However, 6 bits are intended for the calibration process.

The ILO implementation is based on a Colpitts oscillator, enhanced by incorporating a locking mechanism through an injected signal, as shown in Figure 11. This structure enables the oscillator to lock onto an external frequency source, thereby reducing phase noise and enhancing spectral purity.

The ILPS system utilizes the inherent characteristics of the Colpitts oscillator, such as its feedback network consisting of a combination of capacitors (C1, Cvar, and input Balun TR1), to establish a resonant circuit that determines the oscillation frequency, coupled with inductive degeneration (L deg) to achieve higher frequencies. By adjusting the feedback components, the oscillator can be finely tuned to the desired frequency (Figure 12), which is then locked by the injection of a stable reference signal.

The second critical block of the frequency synthesizer is a 2-bit 0/45/90/135° broadband phase shifter centered at 75 GHz to address the two usual frequencies (73 and 77 GHz). This 2-bit phase shifter using switched transmission line technique is shown in Figure 13. It is based on four transmission lines controlled by

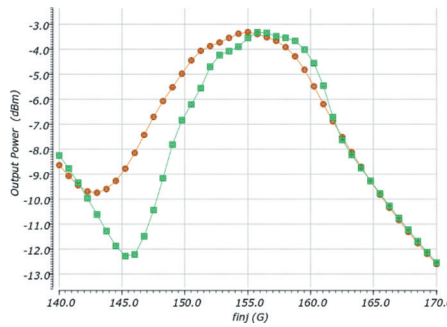

Fig. 12. Tuning of the locking bandwidth.

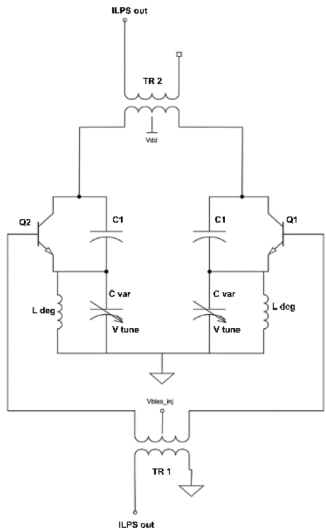

Fig. 11. Colpitt-based ILPS schematic.

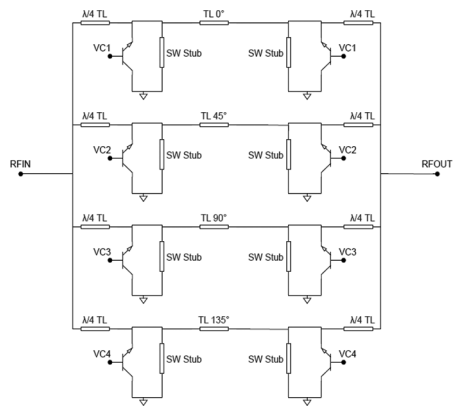

Fig. 13. Switched line phase shifter (SLPS) topology.

two quarter-wave shunt SP4T high-speed bipolar switches to take advantage of the benefits of the B55X technology. Each switched transmission line is sized to provide up to 135° of phase delay in 45° steps (with a maximum phase error of ±3.8° in the bandwidth). This passive architecture (SLPS: switched line phase shifter) was chosen to minimize insertion loss in our specific case (2 bits with a phase shift up to 135°). It is a trade-off between a classic usual passive topology such as SFPS (switched filter phase shifter [15]) that presents high RF losses and a more complex active vector modulator phase shifter type dedicated to 360° phase shift [16]. The power consumption is 7.4 mW. In terms of performance, the phase shifter cell can operate in 73–77 GHz bandwidth and the insertion loss is limited to 3.0 dB with higher than 17-dB return loss.

E. Advanced RF Packaging

The integration of chips and antennas poses a challenge owing to the high operating frequency and wide channel bandwidth. However, realizing the full potential of SiGe BiCMOS and InP advanced technologies demands the utilization of cutting-edge integration concepts. Furthermore, advanced simulation of heat dissipation within the package is imperative.

The Center Core Embedding [11] is developed by AT&S and uses an organic laminate substrate to place monolithic components (e.g., RF chips) within an RF-performant multi-layer printed-circuit board (PCB). As depicted in Figure 14, the monolithic components are first embedded within a core dielectric layer. After this, a stackup of metal and dielectric layers is added on the top and bottom of the core layer.

The monolithic integrated components are connected to the first conductive layers by copper plated micro-vias. Micro-vias have a better conductivity compared to solder bonds or aluminum wire bonds, and introduce smaller inductive and capacitive effects, resulting in lower insertion losses for the high-frequency signals.

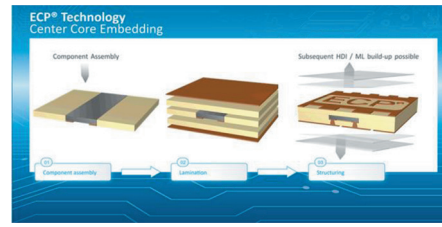

Fig. 14. AT&S Center Core Embedding technology.

The enforcement to integrate chips fabricated using different technologies (BiCMOS and InP) within the same Center Core Embedding presents several challenges. Notably, their thickness must align with the same core layer, and the back-end-of-line (BEOL) finishing of all chips must be compatible with the same micro-via fabrication option. Additionally, the dimensions of the chips are comparable to those of the D-band antenna, posing challenges for floor planning and routing within the RF package itself. These challenges, which are still under study, are pivotal for achieving the functional integrated D-band transceiver envisioned in this project.

F. Antennas in Packaging

The advanced RF packaging technology is essential to ensure a tight and low-loss integration of millimeter-wave integrated circuits (MMICs) and high-efficiency off-chip antennas, as well as an accurate and repeatable manufacturing of the TX and RX module at D-band. The constraints of standard PCB technology, such as the

minimum conductor width (~75 µm) and diameter of the vias (~100 µm), and the related tolerances severely limit the design flexibility and the achievable antenna performance beyond 100 GHz. Among the D-band modules reported in the literature, only the one described in [17] uses a standard PCB technology. The MMIC was flip-chipped using solder bumps on the bottom of the PCB and excited a 2 × 2 cavity-backed microstrip patch array on the top side. A moderate sensitivity of the input impedance of the antenna to the assembly process and relatively high interconnect losses (~1.5 dB) were observed. Similar designs with an external MMIC connected to an antenna-in-package (AiP) were realized using High-density interconnect (HDI) PCB technology [18] and semi-additive processing [19], enabling design features down to 40 and 15 µm, respectively. The matching and gain bandwidth of these antennas are generally less than 15% [19]. With respect to these works, the MMICs will be embedded in the core substrate of TX and RX modules, leveraging on the proposed packaging solution, and directly connected to the antennas, reducing the overall occupied area and the interconnect loss. The radiating elements and part of their feeding structures will be manufactured with several stacked pre-preg layers, each with a thickness of 20 µm, enabling the realization of micro-vias with a 20-µm diameter and a minimum conductor width of 15 µm. A main objective is to limit the number of pre-preg layers, to enhance the robustness and viability of the modules, achieving at the same time a fractional bandwidth of 10% or greater. To this end, several antenna designs are being developed and compared. Different solutions could be optimized for the TX and RX modules, considering the specific integration and performance requirements

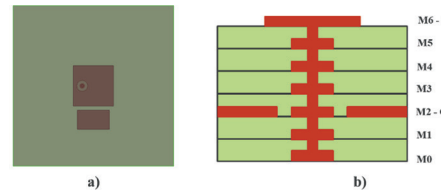

Fig. 15. Probe-fed patch antenna with parasitic: a) top-view of HFSS model, b) cross-section of the antenna stack-up (prepreg layers on top of the core).

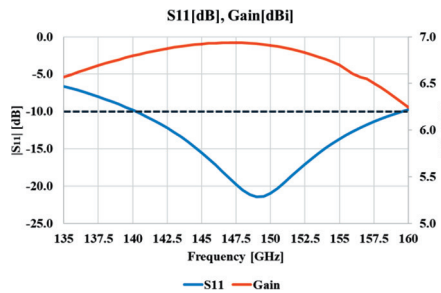

Fig. 16. Simulated S11 and gain of the probe-fed antenna patch with parasitic, in function of frequency.

of each system, as well as the manufacturing capabilities available for the final demonstrators.

Regarding the TX array, a probe-fed patch antenna element has been designed, as part of the initial system-level study. It comprises a single coplanar parasitic radiator to widen the bandwidth. Figure 15a shows the top-view of the simulation model of the design and Figure 15b illustrates the related cross-section, including six 20-µm thick Ajinomoto build-up films, modeled as dielectrics with a relative permittivity of 3.2 and a loss tangent of 0.01. The simulated input reflection coefficient and gain of the stand-alone antenna are plotted in Figure 16 as functions of frequency. The current –10 dB matching bandwidth of the antenna ranges from 140 to 160 GHz with a gain higher than 6 dBi.

In parallel to standard patch antennas, a more complex radiating element,

a magnetoelectric (ME) dipole [20], is under development for the RX system. This antenna generally attains a higher gain and a wider bandwidth with respect to patches, for a given electrical distance between the radiator and ground plane. The technological feasibility of a preliminary ME dipole has been validated. The distance between the printed dipole and the ground plane is 120 µm (six pre-preg layers). The ME dipole is fed by a substrate-integrated waveguide in the core substrate. The simulated peak gain is 8.7 dBi at 156 GHz and the −3 dB gain bandwidth spans from 137.5 to 165 GHz.

An additional design iteration is anticipated for both proposed antennas to enhance the performance of the transmitter (TX) and receiver (RX) antenna arrays, as they are influenced by mutual coupling among the elements and finite-size effects. Furthermore, the RF interconnects from the MMIC through the core substrate, require thorough consideration. Particularly critical is the optimization of these transitions, especially for the InP PAs of the transmitter.

Finally, a second design of the antenna-in-package (AiP) is envisioned to co-optimize the impedance of each antenna element with the impedance of the corresponding input (output) of the RX (TX). This co-design may be greatly beneficial, with respect to standard conjugate matching approaches, to enhance the SNR of the RX module and the scanning range and EIRP of the TX array.

V. CONCLUSION AND OUTLOOK

This work focuses on the development of an innovative transceiver prototype suitable of future generation mobile communication. Leveraging the broad spectral bandwidth beyond 100 GHz, this transceiver targets to utilize two 5-GHz RF channels at D-band, namely 143.5−148.5 GHz and 151.5−156.5 GHz. We aim to demonstrate wireless beamformed links between a TX phased-array front-end and a RX phased-array front-end.

An initial study of the link budget is presented, envisioning LoS communication between a BS and a UE, achieving data rates of up to 30 Gb/s over a distance of 100 m. The specifications derived for the upstream transmission from the UE and downstream reception at the UE guide the circuit design process. However, the final demonstrator aims for a less demanding wireless link scenario. This approach is adopted to mitigate risks and allows us to concentrate on addressing the critical technical challenges associated with technology integration.

The RX uses ST BiCMOS B55X technology while the TX combines chips in ST B55X and III-V-Lab InP technologies. The B55X technology boasts top-of-the-line performance for RF and mixed signal applications on silicon, whereas the InP technology excels in efficient amplification and power delivery beyond 100 GHz. Integration of both TX and RX front-ends will be accomplished within an advanced multi-layer RF packaging, featuring antennas that promise low-loss RF performance at D-band. The proposed circuit topologies for the B55X RX and TX front-ends, as well as for the InP PAs, prioritize RF functionality and efficiency. The antennas are designed on one side of the RF advanced packaging stack-up. The TX RF packaging, integrating both B55X and InP chips with distinct BEOL finishing, demands extra attention.

All these preliminary studies and choices guide the continued chip designs and fabrications. Firstly, the tape-out of critical test structures is planned, including test vehicles for the RF packaging. Subsequently, the design of chips and packaging for the final wireless demonstrator will be executed.

ACKNOWLEDGMENT

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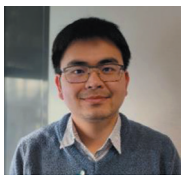

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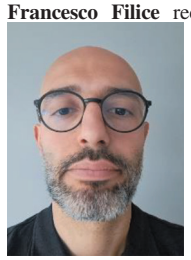

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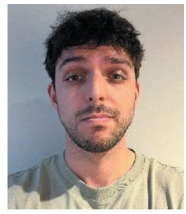

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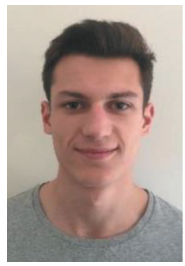

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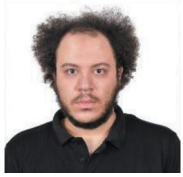

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