D-band Phased Array Antenna Module for 5G Backhaul

A. Fonte, S. Moscato, R. Moro, A. Pallotta, A. Mazzanti, A. Bilato,
G. De Filippi, L. Piotto, F. Centurelli, P. Monsurrò,
H. Sadeghi Chameh, P. Tommasino, A. Trifiletti, D. Lodi Rizzini,
F. Tesolin, S. M. Dartizio, and S. Levantino

Abstract—**The 130–175 GHz frequency spectrum, identified as D-band, will be the key-enabler for next-generation backhauling point-to-point wireless links. Since capacity requirements for mobile networks will increase according to 5G/B5G deployment needs, a new paradigm for radio equipment needs to be developed. Integrated technologies based on silicon-germanium, exhibiting sub-THz cut-off frequency, are going to be adopted to design and implement the key building blocks for fully integrated transceivers. D-band radio frequency integrated circuits and antenna concepts are presented, tailoring phased array allowing electronic beamsteering and beamforming features.**

Index Terms—**5G, antenna array, backhaul, BiCMOS, D-band, low-noise amplifier, phased array, power amplifier, mmWave**

This work is supported by the Chips Joint Undertaking (Chips JU) under grant agreement number 101096256 (project SHIFT). The Chips JU receives support from the European Union's Horizon Europe research and innovation program and the National Authorities.

Alessandro Fonte, Riccardo Moro, and Stefano Moscato are with the R&D Department, SIAE MICROELETTRONICA, Cologno Monzese (MI), Italy (e-mail: alessandro.fonte@siaemic.com).

A. Pallotta is with STMicroelectronics s.r.l., v. Tolomeo, 1 Cornaredo (MI), Italy, A. Mazzanti, A. Bilato, G. De Filippi, and L. Piotto are with the Department of Industrial and Information Engineering, University of Pavia, Pavia, Italy, F. Centurelli, P. Monsurrò, H. Sadeghi Chameh, P. Tommasino, and A. Trifiletti are with Information Engineering, Electronics and Telecommunication Department, Sapienza University of Rome, Italy, D. Lodi Rizzini, F. Tesolin, S. M. Dartizio, and S. Levantino are with the Dipartimento di Ingegneria Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milano, Italy.

I. INTRODUCTION

THE current backhauling systems for mobile telecommunications allow for interconnection of distributed access stations to the core of the network. Wireless backhauling is still a competitive option over fiber optics, especially as multi 10 Gbps capabilities become available. Its share should indeed be maintained with the deployment of 5GNR and 6G, while the overall market will grow thanks to the increased demand for denser networks.

The developments of the technologies and systems carried out with this work aim to overcome the existing limitations and to facilitate the introduction of millimeter-wave (mmWave) telecommunications for the backhauling of telecommunications, replacing the current wireless links. This system is based on the antenna in module (AiM) solution, shown in Figure 1a and 1b, that provide alternative approaches with respect to the standard one (radio frequency integrated circuits (RFICs) and external

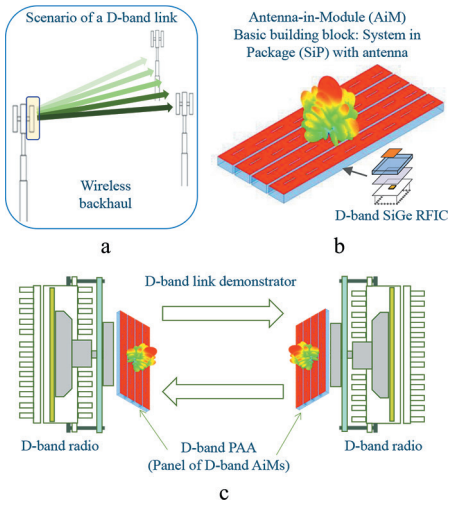


Fig. 1. Scenario of a D-band radio link (a), antenna in module (AiM) basic building blocks (antenna, package, and RFICs) (b), mockup of the D-band radio unit with integrated phased array antenna (PAA) (c).

antenna). Moreover, the AiM as part of a phased array antenna (PAA) increases the total output power through beamforming also allowing the possibility of steering functionality. The D-band AiM concept requires several challenges to be solved, and in particular, (i) at design level, high output power, and low-noise figure at D-bands can be reached, and a very high-integration of the RF front-end is required due to very limited area available for the dies in the PAA, (ii) at the package level, the AiM needs a launcher in the package (LiP) that is necessary for connection to the waveguide antenna.

The advantages of the AiM solutions are (i) the low-cost of the basic component, (ii) the plug and play on other wireless systems (off-the-shelf), and (iii) the reduced design time than any ad-hoc D-band solution.

This paper is organized as follows. In Section II, the D-band system architecture is explained. In Section III, the design of the D-band antenna of the AiM is described, and in Section IV the silicon-germanium (SiGe) RFICs, and in particular the key building blocks of the TX and RX D-band system are described. Finally, in Section V, the conclusions are drawn.

II. D-BAND SYSTEM ARCHITECTURE

The D-band panel of AiM, due to its small size, is expected to be replicated 4 or 8 times on the case of a practical equipment, such that 4 independent beams can be obtained. These can be exploited to offer multibeam equipment or a 2 × 2 MIMO (Multiple-input Multiple-Output) in dual polarization, thus allowing even more capacity and flexibility.

The AiM system will therefore enable the transition of backhauling/midhauling/fronthauling wireless links for 5G and future evolutions. The envisioned system architectures for communication systems involving the AiM are shown in Figure 1c. The relevant aspects of such architectures with the AiM components are: (i) the system designer should only be concerned with the core aspects of its application, such as data gathering, processing, user interaction, and can ideally effortlessly place the AiM components without dealing with mmWave RFICs design, (ii) the circuit designer should not be concerned by critical RF interconnections, which may often require a longstanding experience in the field (all connections needed are baseband ones), (iii) the device will not need an external antenna, as it is included into AiM components, and (iv) the application can rely on very-high-speed communications allowed by the usage of mmWaves and transparently handled by the AiM.

The AiM fully integrated module includes four TX/RX mmWave chains, designed in SiGe BiCMOS process,

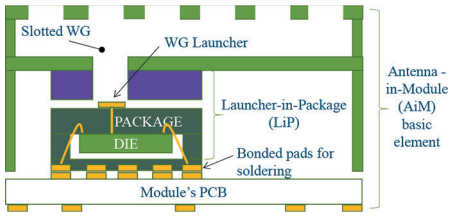


Fig. 2. First design of D-band AiM assembly.

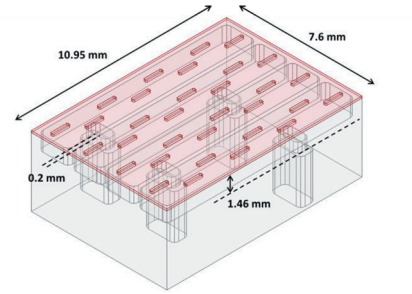


Fig. 3. Slotted waveguide D-band antenna structure.

together with biasing and control sections. For each chain, an LiP is required to feed the antenna located on the top of the structure. The aim of this architecture is to reach a very high level of integration that permits to reduce interconnection losses and to increase the system efficiency. Moreover, the module described exhibits all the characteristics of an active phase array since a proper tuning of the input signal can be performed. The phase and amplitude can be changed independently by the four mmWave chains to implement beamforming and beam-steering features. The first design of AiM assembly, shown in Figure 2, presents all the building blocks necessary to implement the D-band module.

Looking at the architecture, two main areas can be highlighted; the active components, i.e., the RFICs, and the antenna, whose characteristics and performance are described in the next sections.

III. ANTENNA-IN-MODULE DESIGN

The radiating structure and its integration in the AiM are important to limit the signal loss and to permit the scan of the beam, reducing the drawbacks tied to this approach (gain loss, grating lobes, etc.). In addition, a critical aspect to face in the antenna design is the size that cannot be excessive to keep the module replicable in more complex systems such as a MIMO configuration.

After a first analysis of several solutions presented in literature [1] and by converting the requirements described in an antenna typology, four in-line antenna arrays with a planar dimension limited to 8 × 16 mm^2 have been identified. The feeding points are positioned far away from each other to accommodate the RFICs. In terms of electrical performance, the antenna works in the D-band and has a minimum operating bandwidth of 10 GHz, which allows to address the maximum D-band channels bandwidth of 5 GHz and 20 dBi of minimum overall gain.

Among the different designs that meet those constraints, the most suitable one to guarantee good performance is based on the hollow metallic waveguide technology. An example that was developed and that can be used as an antenna reference for this system is the slotted waveguide antenna array shown in Figure 3. The structure consists of four blocks of eight radiating elements, which are linear slots etched in the waveguide top metal layer. The number of slots chosen allows reaching a gain high enough while keeping the tight dimensions but with the disadvantage of a narrow operating bandwidth. The position of the radiating elements was studied to achieve broadside linear polarized radiation at 145 GHz. Furthermore, the slots on the top layer together with

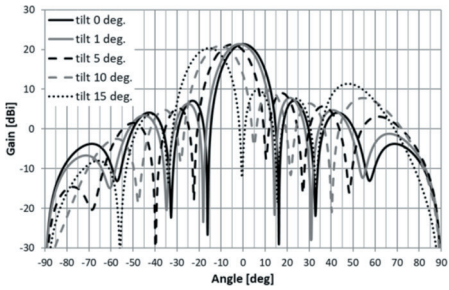


Fig. 4. Antenna radiation pattern for different steering angles.

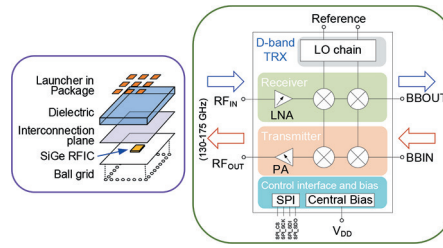


Fig. 5. Mockup of the package and the simplified building block scheme of the SiGe BiCMOS TRX RFIC.

the matching section in the feeding waveguide were optimized to guarantee an input return loss better than 15 dB.

The antenna array was simulated exciting the four input waveguides (standard WR6) in-phase. A 15 dB return loss is obtained over a bandwidth of 12 GHz (8% relative bandwidth). The input matching behavior is similar for all the ports showing that the impact of mutual couplings between the slots is negligible. At center frequency of 145 GHz, the antenna gain is 21.38 dBi. The simulation results confirm that the design presented is in line with the application requirements and it can be used as a reference for other structures that aim to improve its limitations. A wider bandwidth, for example, would be an added value also to have a margin for the manufacturing mechanical tolerances.

The presented structure has also beamsteering capability, which can be exploited to compensate for the misalignment and to simplify the deployment of the link. To verify the performance of the antenna for a displacement of a few degrees of the main lobe direction, a progressive phase on the consecutive ports was applied for different phase values. In Figure 4, the resulting E-plane radiation pattern is shown. Applying a phase shift of 10° between the four antennas, the main lobe is steered by 1.6° with a scan loss of 0.015 dB.

IV. D-BAND SIGE RFICS

This section presents the technology process selected for this project and some key active components of the D-band AiM: the power amplifier (PA), D-band mixers, the low-noise amplifier (LNA) and the low-phase-noise local oscillator (LO). A mockup of the package and the simplified building block scheme of the TRX RFIC are shown in Figure 5.

A. Improved SiGe:BiCMOS HBT and Back-End Process

The SiGe:BiCMOS technology has been proven as a viable and enabling technology for beyond 100 GHz mmWave front-end modules, by fully exploiting the flexibility and the integration capabilities envisioned by mixing digital and analog functionalities. SiGe Heterojunction Bipolar Transistor (HBT) architecture evolved significantly over the years with the objective of always improving (shrinking) the vertical profile (driving f_T) and reducing the parasitics (base resistance R_B and collector–base capacitance C_{BC} being critical for f_{MAX}). The exploitation of the radio spectrum in D-band (130–174.8 GHz), by relying on power-efficient RFIC chipset for an active phased antenna array system with beamsteering functionality, has been made feasible by an advanced

SiGe:BiCMOS process, based on a nine-metal stack back-end option and HBT structure having f_T and f_{MAX} > 400GHz.

The main concept behind the new process recipe is the use of a mono-crystalline base link between intrinsic SiGe base and the external base electrode to minimize the base resistance of the SiGe HBTs. Developments at STMicroelectronics started from the 55 nm BiCMOS platform currently in production, in which the high-speed SiGe HBT features 320 GHz f_T and 370 GHz f_{MAX}. The final objective is to offer a 400 GHz f_T and 500 GHz f_{MAX} HBT on the same CMOS node. Three major process changes are implemented to reach this objective [2]:

- The first one is the modification of the process thermal budget with the reduction of the spike annealing temperature and the addition of a millisecond annealing. It allows to increase the f_T of the SiGe HBT thanks to a reduction of dopants diffusion and a better activation of these dopants. Process conditions have also been defined to not degrade the performances of the CMOS transistors.
- The second change applies to the extrinsic collector module with the replacement of the buried layer by an implanted collector, which reduces both the cost and the cycle time of the technology. Super Shallow Trench Isolation (SSTI) is implemented to reduce the base–collector capacitance.
- Finally, a STMicroelectronics proprietary SiGe HBT architecture, called EXBIC (for Epitaxial eXtrinsic Base Isolated from the Collector), is being developed to address the f_{MAX} challenge. The key feature of this architecture is a boron in-situ doped epitaxial base link used to reduce the extrinsic base resistance.

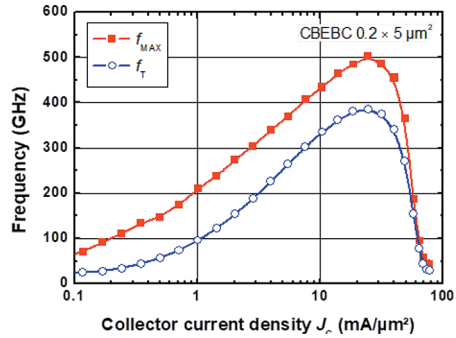


Fig. 6. Measured RF-performance (dots) versus SPICE model simulation (solid lines).

Measured RF-performances (f_T and f_{MAX}.vs. collector current density) are shown in Figure 6.

Besides the high-speed performances of the HBT, the nine-metal back-end of line (BEOL) has been adjusted to increase the Q-factor of inductors and reduce the attenuation constant of transmission lines (TLINEs). This is achieved by implementing two thick Cu layers for the vias (2.7 µm wide) and for the lines (2.3 µm wide) available in 300 mm wafers.

B. Heterodyne D-Band TX Front-End

The building block scheme of the transmission section of the D-band SiGe RFIC is shown in Figure 5. The two building blocks, i.e., the PA and the up-conversion mixer, were developed and validated in the STMicroelectronics 55 nm BiCMOS process and then redesigned in the new process with enhanced HBT transistor (i.e., the B55X process).

The D-band PA, whose circuit schematic is shown in Figure 7a, comprises HBTs in common base (CB) and a cascode input stage to rise the overall gain [3]. The CB configuration is selected, in most of the stages, giving its higher power and efficiency compared to the common emitter one. The HBTs area is scaled progressively along the chain,

starting from the output stage that is sized to deliver a saturated power $P_{sat} > 17$ dBm. To improve the efficiency in back-off, the quiescent current is set low, such that the average current expands with the signal leveraging the current clamping mechanism, enabled by the CB stages with a DC-feed inductance from the emitter terminals to ground [4]. The matching networks are realized with TLINEs, allowing simpler and more reliable modeling of the return signal paths than spiral inductors, a critical issue in D-band. The TLINEs are shielded microstrips, with the signal in the topmost copper metal layer. The geometrical parameters (widths and spacings) are optimized to minimizing the TLINEs insertion loss.

Looking at the schematic of the up-conversion mixer in Figure 7b, [5], the transformer T_1 provides input matching for the IF cascode amplifier ($Q_{1,2}$–$Q_{3,4}$). The LO input is buffered with a single-ended cascode ($Q_{5,6}$) and made differential by T_3. The switching-quad ($Q_{7,8}$–$Q_{9,10}$) is fully balanced for LO suppression. It is found that a major limitation to the mixer output power stems from the low output resistance of the switching quad, reduced in D-band by the feedback of the HBTs Miller capacitors and the extrinsic base resistors. $Q_{11,12}$ are thus stacked to the switching quad to raise the output impedance and increase P_{out}. T_3 combines the output currents into a single-ended D-band signal. The HBTs in the switching quad, with emitters grounded by the secondary inductance of T_3, operate in CB for the IF signal. Thus, in the same way as in the PA, current clamping is exploited to expand the average current with the signal and maintain good efficiency in power back-off. The transformers T_1–T_4 are realized as coplanar windings in the topmost metal layer.

Photographs of PA and mixer in the BiCMOS-55 nm technology are shown in Figures 8 and 9, together with a measurement summary. The PA demonstrated 17.6 dBm P_{sat} with 2.2 V supply at 135 GHz. The small-signal gain is 24 dB with P_{out} at 1dB gain compression is P_{1dB} = 16.8 dBm, ~1dB below P_{sat}. The DC current rises from 30 mA at the quiescent point to 130 mA at P_{1dB}. The peak power-added efficiency (PAE) is 17.5% and still 8.5% at 6 dB power back-off. The mixer, with an IF signal at 40 GHz and –3 dBm LO at 100 GHz, achieved 15 dB conversion gain with RF and IF bandwidths of 38 and 15 GHz, respectively. The measured P_{sat} = 6.3 dBm and P_{1dB} = 4.5 dBm are remarkably high. The DC current rises from 34 mA at the quiescent point to 66 mA at P_{1dB}.

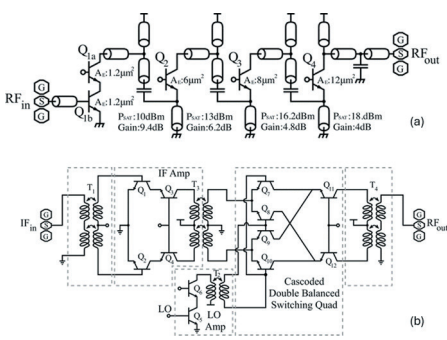
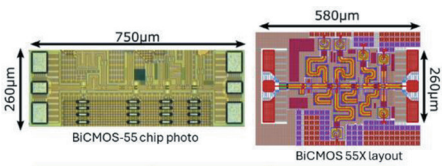
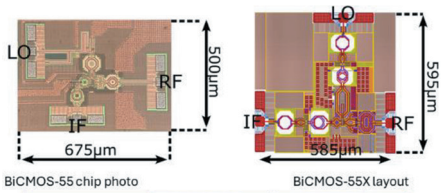


Fig. 7. Schematics of the D-band PA (a) and heterodyne up-conversion mixer (b).



	BiCMOS – 55nm (measurements)	BiCMOS - 55X (Simulations)
Supply [V]	2.2	2
-3dB BW [GHz]	[125 - 159]	[110 – 175]
Gain [dB]	24	19
P_{SAT} [dBm]	17.6	[16.8 –19.8]
P_{1dB} [dBm]	16.8	[16.0 –19.5]
PAE [%]	17.5	[10.5-15.5]
PAE @ 6dB BO [%]	8.5	7

Fig. 8. D-band PA. Chip photograph in 55 nm BiCMOS, layout view in the new B55X process and performance summary and comparison.



	BiCMOS – 55nm (measurements)	BiCMOS - 55X (simulations)
Supply [V]	2	2
-3dB RF-BW [GHz]	[112 - 150]	[126 – 175]
-3dB IF-BW [GHz]	[32-47]	[54-88]
LO power [dBm]	-3	-2
Conv-Gain [dB]	15	18.5
P_{SAT} / P_{1dB} [dBm]	6.3 / 4.5	6.8 / 5.5
η @ P_{1dB} [%]	2.5%	5.4%

Fig. 9. D-band up-conversion mixer. Chip photograph in 55 nm BiCMOS layout view in the new B55X process and performance summary and comparison.

The PA and mixer have been redesigned with performances adjusted to the target application, taking benefit of the advanced B55X process. The layout of the chips and the performance summary from post-layout simulations are reported in Figures 8 and 9. The layout of the PA was optimized with 25% reduced footprint. The gain is purposely reduced to 19 dB, considering the high P_{out} available from the mixer. Thanks to the higher HBTs f_T/f_{max}, the bandwidth is extended to 110–175 GHz, allowing to cover the full D-band with a single component. The expected P_{out} is comparable or slightly better than in the 55 nm BiCMOS design. The IF of the mixer is shifted to E-band and the operation bandwidth (both at RF and IF) is remarkably increased. The higher HBTs gain is exploited to raise the conversion gain with nearly the same P_{out} but remarkably higher expected efficiency.

C. Heterodyne D-Band RX Front-End

The receiving section of the D-band RFIC includes two D-to-E-band down-converters (D/C): a low-band (130–150 GHz) D/C and a high-band (150–165 GHz that can be extended to 175 GHz), which allow covering the overall D-band. The full D-band receiver will be obtained by cascading the D-band D/C stage to an E-band receiver already designed in 55 nm BiCMOS technology [6] and presently under design in the new B55X process.

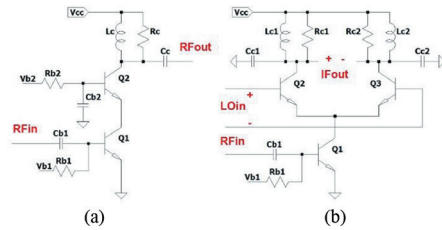


Fig. 10. Simplified schematic of the LNA core (a) and of the D/C mixer core (b).

The two RFICs implementing the two D/C blocks have been designed in B55X technology. They share the same architecture and circuital topology: they are composed of two building blocks, a two-stage D-band LNA and a single-balanced D/C mixer based on an active two-quadrant analog multiplier. The two above-mentioned building blocks have been also taped-out as stand-alone RFICs in the two sub-bands for testing purpose.

The core of the single-stage LNA has been designed exploiting a cascode topology, as shown in the simplified circuit schematic of Figure 10a: the load inductor is implemented with a minimum-width microstrip line, provided by the Process Design Kit (PDK). The cascode stage bias current has been chosen in order to guarantee a low-noise Figure (< 8 dB) over the whole bandwidth, but without sacrificing the linearity performance (output P_{-1dB} approaching 0 dBm), according to the state-of the-art of D-band BiCMOS LNAs [7].

Two versions of the LNA have been designed, the second one with the goal to increase the gain up to at least 20 dB.

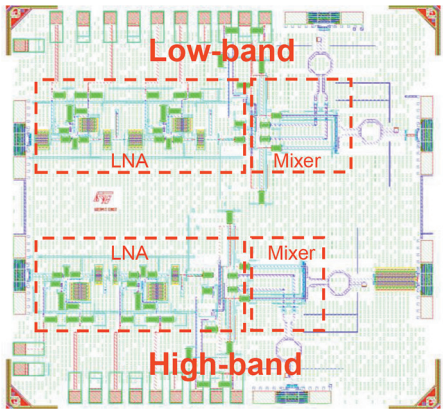


Fig. 11. Layout of the fabricated D-band to E-band D/Cs.

TABLE 1.
SIMULATED PERFORMANCE OF D-BAND BLOCKS.

	Gain [dB]	NF [dB]	OP_{1dB} [dBm]
Low-band LNA 1	17.5	6.6	−1.0
Low-band LNA 2	21.6	6.6	−3.4
High-band LNA 1	14.9	7.4	−2.0
High-band LNA 2	20.0	7.4	−3.5
Low-band mixer	−3.2	18.0	−4.2
High-band mixer	−5.5	23.0	−13.3
Low-band down-converter	14.0	7.6	−12.1
High-band down-converter	11.9	9.2	−13.0

The core of the down-conversion mixers, shown in Figure 10b, is a differential pair with a tuned *R-L-C* load. The tuned load is composed of a minimum-width microstrip line and a metal-oxide-metal (MOM) RF capacitor. For both the LNA and the mixer building block, the matching networks have been designed exploiting a single-stub topology: a microstrip line allows matching to 50 Ω of the real part. The remaining reactive part is cancelled by means of a grounded MOM capacitor or inductor (again implemented by using a minimum-width microstrip line). Finally, baluns have been used at the LO input and at the E-band IF output. Electro-magnetic post-layout simulations have been performed by Cadence EMX CAD tool to tune loads and matching networks, and also to evaluate effects of interconnections.

In Figure 11, the layout of the test chip containing the two D/C blocks is shown. The total area is 1.4×1.2 mm^2.

In Table I, post-layout simulation results are presented at the center of the bandwidth, i.e., 140 GHz for the low-band blocks and 157.5 GHz for high-band blocks. Simulated S-parameters and noise figure of the high-band LNA are shown in Figure 12.

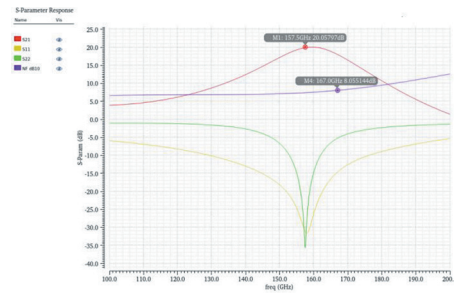


Fig. 12. Simulated S-parameters and noise figure of the high-band LNA.

D. Low-Phase-Noise LO Generator

The LO generator is intended to provide the LO signal to the D-band receiver. Considering the low-band D/C block with an input frequency in the 130–150 GHz range, an LO frequency spanning from 60 to 80 GHz allows to down-convert the signal to an IF frequency of 70 GHz. Frequency generation at mmWave is particularly challenging when low phase noise and wide tuning range (TR) are targeted. The straightforward way to generate a LO would be the direct frequency synthesis from a reference crystal oscillator by means of a phase-locked loop (PLL). However, the relatively low-quality factor of tunable resonators integrated on silicon substrates makes this solution

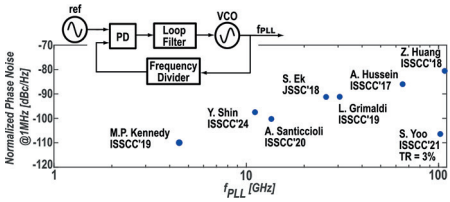


Fig. 13. Direct LO synthesis approach: block diagram of the LO generator and plot of the phase noise at 1 MHz offset from the carrier (normalized at 80 GHz) versus the VCO resonance frequency.

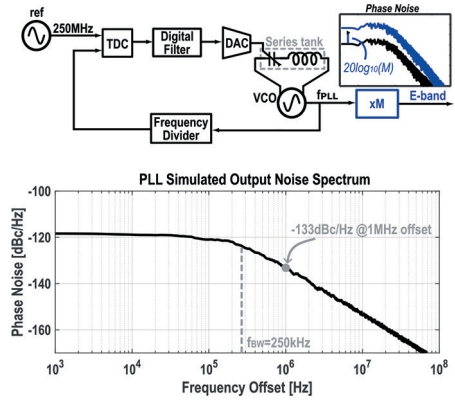


Fig. 14. Indirect LO synthesis approach through a DPLL (with series-resonance VCO) followed by a frequency multiplier, and simulated PLL spectrum.

impractical. This is evident looking at the state-of-the-art of PLL-based frequency synthesizers, whose phase noise presents a worsening trend as the voltage-controlled oscillator (VCO) resonance frequency f_{PLL} increases, as described by the plot of the PLL phase noise at 1 MHz offset from the carrier (normalized at a carrier frequency of 80 GHz) as a function of f_{PLL}, in Figure 13. The outlier is the work in [8], which achieves excellent phase-noise performances at an extremely narrow TR that would be impractical.

Therefore, an indirect frequency synthesis approach is typically preferred at mmWave, in which a PLL is followed by a frequency multiplier. The impact of the frequency multiplication stage on the output phase noise is simply an increase of the PLL phase noise level by . The adoption of frequency multipliers introduces other challenges related to their power consumption and harmonic rejection. In fact, the output of the multipliers contains the sub-harmonics of the output sinusoid. In this work, a good compromise is found by adopting a fractional-N PLL with an output frequency in the 10–13.33 GHz range and a 250 MHz reference signal (so that the PLL frequency division is limited to a factor comprised between 40 and 53.33), followed by a sextupler (performing a sixfold frequency multiplication) to get a local oscillation in the 60–80 GHz range. As shown in the block diagram in Figure 14, the PLL adopts a digital PLL (DPLL) architecture based on a time-to-digital converter (TDC) used as a phase detector to convert the time error between the reference signal and the one coming from the frequency divider into a digital word that is fed to a digital loop filter. The output of the filter is then converted to a voltage by means of a digital-to-analog converter (DAC) driving the VCO tuning voltage. DPLLs offer the big advantage of replacing the analog loop filter with a digital one, with great benefit in terms of area occupation (especially at narrow PLL bandwidths) and configurability [9].

Conventional VCOs based on parallel LC resonators have a voltage swing limited by transistor's breakdown. So, reaching ultra-low phase noise requires increasing power consumption by reducing the resonator impedance or, in other words, by decreasing the inductance L and increasing the capacitance C. However, this strategy has a limit that is reached when L is so small that becomes comparable with the parasitic inductance connecting the varactors. To overcome this limitation, the VCO adopts a configuration based on an integrated LC series resonator and HBT transistors, which has been recently introduced in [10]. This

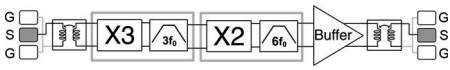


Fig. 15. Block diagram of the frequency sextupler.

solution allows to raise the power delivered to the resonator by increasing the current swing, with no need to scale down *L*. The VCO, designed in BiCMOS-55X process, has a 10–11.5 GHz (14%) TR, and reaches a simulated phase noise of −136 dBc/Hz at 1 MHz offset, with a DC power of 380 mW. A second VCO will be alternatively used to cover the remaining TR. Figure 2 shows the simulated output spectrum of the overall PLL, including the phase noise of reference buffer, TDC, DAC, and frequency divider. The PLL bandwidth f_{BW} of about 250 kHz is chosen to minimize the integrated rms phase noise, which is of about −63 dBc (equivalent to an absolute jitter of 16 fs rms), while the phase noise at 1 MHz offset at the PLL output is of − 133 dBc/Hz.

The sextupler is implemented in B55X as the cascade of a tripler and a doubler, as shown in Figure 15. The two blocks adopt the circuit topology disclosed in [11]. The sextupler achieves, from post-layout simulations, a harmonic rejection better than 29 dB across the output frequency range from 60 to 78 GHz. It has a DC power consumption of 67.3 mW and an area occupation of 0.32 mm^2. The simulated phase noise at the output of the cascade of the PLL and the sextupler is about −117 dBc/Hz at 1 MHz offset.

V. CONCLUSION

The advancement on the development of the basic element of the D-band (130–174.8 GHz) PAA system, called AiM, has been presented. The system architecture, the mockup of the module and the package, the D-band antenna concept, and the RFICs developed by using the cutting-edge STMicroelectronics 55 nm and 55X SiGe BiCMOS technologies have been described and the first results have been shown.

The D-band antenna has been designed to achieve broadside linear polarized radiation at 145 GHz, 15 dB return loss over a bandwidth of 12 GHz, and a gain greater than 20 dBi. Regarding the transmitter section, simulations (in SiGe B55X process) and measurement (in 55 nm SiGe BiCMOS process) results have shown that the D-band PA can achieve power gain > 19 dB, P_{SAT} > 17 dBm and PAE between 10.5% and 17.5%. The D-band up-conversion mixer can achieve conversion gain > 15 dB, P_{SAT} > 4.5 dB, and an operating bandwidth covering the whole D-band. Regarding the receiver section, simulation results (in SiGe B55X process) have shown that the D-band LNA can achieve power gain > 15 dB, noise figure better than 7.4 dB and OP1dB > −4 dBm. The D-band down-conversion mixer can achieve conversion gain > 12 dB, noise figure < 9.2 dB and OP1dB > −13 dBm. The LO generator designed in BiCMOS-55X process includes a PLL and a sextupler: the VCO reaches a 10–11.5 GHz TR and a simulated phase noise of −136 dBc/Hz at 1 MHz offset with a DC power of 380 mW, while the sextupler has a bandwidth from 60 to 78 GHz with a DC power of 67 mW.

REFERENCES

[1] M. de Kok, A. B. Smolders and U. Johannsen, “A Review of Design and Integration Technologies for D-Band Antennas,” in IEEE Open Journal of Antennas and Propagation, vol. 2, pp. 746–758, 2021, doi: 10.1109/OJAP.2021.3089052.

[2] P. Chevalier et al, “B55X: A SHIFT in STMicroelectronics BiCMOS Technologies”, 2024 19th European

Microwave Integrated Circuits Conference (EuMIC), Paris, France, 2024.

[3] I. Petricli, D. Riccardi and A. Mazzanti, "D-Band SiGe BiCMOS Power Amplifier With 16.8dBm P-dB and 17.1% PAE Enhanced by Current-Clamping in Multiple Common-Base Stages," in IEEE Microwave and Wireless Components Letters, vol. 31, no. 3, pp. 288–291, March 2021, doi: 10.1109/LMWC.2021.3049458.

[4] E. Rahimi, J. Zhao, F. Svelto and A. Mazzanti, "High-Efficiency SiGe-BiCMOS E-Band Power Amplifiers Exploiting Current Clamping in the Common-Base Stage," in IEEE Journal of Solid-State Circuits, vol. 54, no. 8, pp. 2175–2185, Aug. 2019, doi: 10.1109/JSSC.2019.2909475.

[5] A. Bilato, I. Petricli and A. Mazzanti, "SiGe BiCMOS D-Band Heterodyne Power Mixer With Back-Off Efficiency Enhanced by Current Clamping," in IEEE Solid-State Circuits Letters, vol. 7, pp. 2–5, 2024, doi: 10.1109/LSSC.2023.3332766.

[6] G. Amendola, L. Boccia, F. Centurelli, P. Chevalier, A. Fonte, C. Mustacchio, A. Pallotta, P. Tommasino, A. Traversa, A. Trifiletti, 'Compact E-Band I/Q Receiver in SiGe BiCMOS for 5G Backhauling Applications,' IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 9, Sept. 2021.

[7] G. De Filippi, L. Piotto, A. Bilato, and A. Mazzanti, 'A SiGe BiCMOS D-band LNA with gain boosted by local feedback in common-emitter transistors,' In 2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp. 133–136, San Diego, CA, USA, 11-13 June 2023.

[8] S. Yoo et al., "23.4 An 82fsrms-Jitter and 22.5mW-Power, 102GHz W-Band PLL Using a Power-Gating Injection-Locked Frequency-Multiplier-Based Phase Detector in 65nm CMOS," in 2021 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021, pp. 330–332, doi: 10.1109/ISSCC42613.2021.9365956.

[9] M. Mercandelli, L. Grimaldi, L. Bertulessi, C. Samori, A. L. Lacaita and S. Levantino, "A Background Calibration Technique to Control the Bandwidth of Digital PLLs," IEEE Journal of Solid-State Circuits, vol. 53, no. 11, pp. 3243–3255, Nov. 2018, doi: 10.1109/JSSC.2018.2866454.

[10] A. Franceschin, D. Riccardi and A. Mazzanti, "Ultra-Low Phase Noise X-Band BiCMOS VCOs Leveraging the Series Resonance," IEEE Journal of Solid-State Circuits, vol. 57, no. 12, pp. 3514–3526, Dec. 2022, doi: 10.1109/JSSC.2022.3202405.

[11] M. M. Pirbazari and A. Mazzanti, "E-Band Frequency Sextupler With >35 dB Harmonics Rejection Over 20 GHz Bandwidth in 55 nm BiCMOS," IEEE Journal of Solid-State Circuits, vol. 57, no. 7, pp. 2155–2166, July 2022, doi: 10.1109/JSSC.2022.3146730.

Alessandro Fonte received M.S. and Ph.D. degrees in electronic engineering from the University of Pisa, Italy, in 2005 and 2008, respectively. Since 2011, he has been with the SIAE MICROELETTRONICA S.p.A. (Milan, Italy), where he is a senior microwave engineer and member of the technical staff. His current research interests include the design of micro- and millimeter-wave system-on-chip front-ends in silicon and III-V semiconductor technologies for point-to-point radio link applications. He has authored several papers in peer-reviewed international journals and conference proceedings and two book chapters. He is the SIAE contact person for European and ESA projects.

Stefano Moscato (S'12) was born in Pavia, Italy, in 1988. He received the Ph.D. degree in electronics engineering from the University of Pavia, Italy, in 2016. He was a visiting Ph.D. student at Georgia Tech, Atlanta, GA, USA, in early 2015. He became part of the R&D microwave group of SIAE MICROELETTRONICA in May 2017. His research activities have been

focused on RF-to-mmWave passive components. Since September 2022, Dr. Moscato has been the coordinator of the 1337 R&D group devoted to the design and validation of mmWave passive components, antennas, and sub-systems. He is involved in innovation programs and founded research for microwave backhauling, O-RAN equipment, and space-oriented assemblies. He was a recipient of an IEEE MTT-S undergraduate/pre-graduate scholarship in 2012. He is the author of more than 50 papers on international journals and conferences. He has been the Chair of the IEEE Student Branch, University of Pavia, from 2013 to 2016.

Riccardo Moro received the M.S. and the Ph.D. degrees in electronic engineering in 2010 and 2013, respectively, from the University of Pavia, Italy. In 2014, he was post-doc researcher at the same university. His main activity was focused on the design of planar components and antennas for radiofrequency applications. From 2015 to 2022, he worked in both consulting firm and telecommunication companies where he gained experience in technical management and analysis of microwave systems. In 2022, he joined SIAE MICROELETTRONICA as a senior RF engineer and he is involved in products development as well as in R&D funded projects.

Andrea Pallotta received the M.S. degree in electronic and telecommunication engineering from the University of Ancona, Italy, in 1990. After about one year period within the University of Ancona as a grant researcher, from 1991 to 1999, he has been with the Optoelectronic R&D Lab of Italtel, involved in many national and European projects as a senior designer. From 1998 to 2000, he was with the SDH Cross-Connect competence center of Siemens as responsible for the Advanced Development Department. He joined the ST end of 2000 as Design and Project Manager by leading the Optoelectronic and High Frequency Lab. His work has included the design and development of optoelectronic modules, GaAs MMIC, Bipolar, BiCMOS, and BCD-based silicon RFICs for high-speed data link, RF power amplifiers, and RF transceivers. He is leading, for more than 20 years, both product development and coordination activities of several European R&D funded projects in the field of the optoelectronic and RF telecommunication systems. He is the author and co-author of 19 technical papers and holds 15 patents.

Andrea Mazzanti received the Laurea and Ph.D. degrees in electrical engineering from the University of Modena and Reggio Emilia, Modena, Italy, in 2001 and 2005, respectively. During the summer of 2003, he was with Agere Systems, Allentown, PA, as an Intern. From 2006 to 2009, he was an assistant professor with the University of Modena and Reggio Emilia. In January 2010, he joined the University di Pavia, where he is currently a full professor of electronics and the scientific director of a joint lab between University and STMicroelectronics. His main research interests cover device modeling and IC design for high-speed communications, RF, and millimeter-wave systems. Dr. Mazzanti was a member of the Technical Program Committee of the IEEE Custom Integrated Circuit Conference (CICC), European Solid State Circuits Conference, and International Solid State Circuits Conference (ISSCC). He was an associate editor for the Transactions on Circuits and Systems and IEEE Solid-State Circuits Letters and a Guest Editor for a number of special issues of the Journal of Solid State Circuits. He currently serves as a Distinguished Lecturer of the IEEE Solid-State Circuits Society.

Andrea Bilato received the B.S. degree in information engineering, M.S. degree in electronic engineering, and the Ph.D. degree from the University of Padua, Padua, Italy, in 2015, 2017, and 2021, respectively. During his Ph.D., from 2019 to 2020, he was an intern with Infineon Technologies AG, Munich, Germany, where he worked on transceiver front-end circuits for radar systems operating beyond 100 GHz. Since 2021, he has been a post-doctoral researcher with the Department of Industrial and Information Engineering, University of Pavia, Pavia, Italy. His current research interests include the IC design of D-band transceiver building blocks for wireless high-speed communications.

Lorenzo Piotto was born in Padua, Italy, in 1994. He received the B.Sc. and M.Sc. degrees in electronics engineering from the University of Padua, Padua, Italy, in 2016 and 2018, respectively.

From 2019 to 2020, he was with Infineon Technologies Austria, Villach, Austria, where he worked on the design

and verification of mmWave blocks for wireless communication. In 2021, he joined the University of Pavia where he is working toward his Ph.D. His current research interest is in the design of building blocks for high-data-rate backhaul communications operating in D-band.

Guglielmo De Filippi was born in Milan, Italy, in 1993. He received the B.Sc. and M.Sc. degrees in electronics engineering from Politecnico di Milano, Italy, in 2017 and 2020, respectively, and the Ph.D. degree in microelectronics from the University of Pavia, Italy, in 2024.

In 2019, he was a thesis student with the ARP Laboratory, Politecnico di Milano, where he focused on mmWave building blocks for E-band wireless communications. In 2020, he joined the AIC Laboratory with the University of Pavia, Pavia, Italy. His current research interest is in D-band building blocks for high-data-rate wireless backhaul communications and radars.

Francesco Centurelli was born in Roma, in 1971. He received the laurea degree (cum laude) and the Ph.D. degree in electronic engineering from the University of Roma "La Sapienza", Roma, Italy, in 1995 and 2000, respectively. In 2006, he became an assistant professor with the DIET Department of the University of Roma La Sapienza. His research interests were initially focused on system-level analysis and design of clock recovery circuits and high-speed analog integrated circuits, and now concern the design of analog-to-digital converters and very-low-voltage circuits for analog and RF applications. He has authored or co-authored more than 100 papers on international journals and refereed conferences, and has been also involved in R&D activities held in collaboration between Università "La Sapienza" and some industrial partners.

Pietro Monsurrò was born in Rome, Italy. He received the Ph.D. degree in electronic engineering from the Department of Electronic Engineering, University of Roma "La Sapienza," Italy, in 2008. He is currently an associate professor with the Department of Information Engineering, Electronics and Telecommunications of the University of Roma "La Sapienza," Italy. His current research interests include low-voltage low-power analog and mixed-signal circuits in advanced CMOS processes, analog filter design in CMOS and BiCMOS processes and filter synthesis techniques, behavioral models of mixed-signal and RF systems, digital background calibration techniques for pipeline, and time-interleaved analog-to-digital converters, including advanced time-interleaved architectures, model identification, and adaptive algorithms.

Hassan Sadeghi Chameh received the master's degree in communication engineering with the Cardiff University and is currently studying the Ph.D. degree in electronic engineering with the University of Roma "La Sapienza." His research interests are in the design of integrated circuits for E-band and D-band transceivers.

Pasquale Tommasino received the master's degree in electronic engineering and the Ph.D. degree from the University of Roma "La Sapienza" in 1992 and 1999, respectively. Since 1995, he has been with the Electronic Engineering Department (now Department of Information Engineering, Electronics and Telecommunications) of the University of Roma "La Sapienza," where since 2007 he has been an assistant professor. His research interests are mainly oriented to the design of RF and microwave broadband circuits. Presently, he is mainly engaged in the design of integrated circuits for E-band and D-band transceivers.

Alessandro Trifiletti was born in Rome, Italy, on October 4, 1959. In 1991, he joined the Electronic Engineering Department of "La Sapienza" University in Rome as a research assistant, where he was involved in research activities dealing with analogue, RF, and microwave IC's design. In 2001, he became an assistant professor and in 2005, he got the position of Associate Professor and in 2019 the position of Full Professor at the Engineering Faculty of the same university. Prof. Trifiletti has worked in the

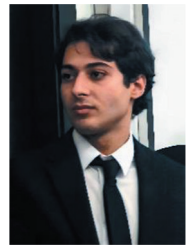
field of microelectronics, both from the point of view of design methodologies and circuit topologies. On these subjects, Prof. Trifiletti has (co-) authored over 210 publications, of which about 80 published on international journals, the others published on the proceedings of major international conferences (a large part of these sponsored by the IEEE). He is presently a reviewer for some IEE and IEEE reviews, among them: IEEE Transactions on Microwave Theory and Techniques, IEEE Transactions on Circuit and Systems (parts I and II), IEE Proceedings on Circuits, Devices and Systems, and IEE Electronic letters. In the last 20 years, he has been engaged in the coordination of research teams from DIET (previously DIE) in the framework of national and international programs, involving both industrial and academic partners. From an industrial perspective, Prof. Trifiletti's expertise covers topics about analogue and RF microelectronics, Radar and Electronic Support Measures (ESM) systems, high-speed communication systems, security issues in cryptographic algorithms implementation, and embedded system design.

Daniele Lodi Rizzini was born in Casalmaggiore, Italy, in 1999. He received the B.Sc. and M.Sc. degrees in electronics engineering from the Politecnico di Milano, Milan, Italy, in 2021 and 2023, respectively, where he is currently a research assistant.

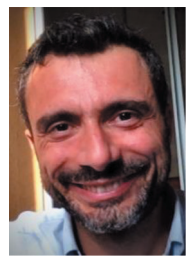
His current research interests include low jitter fractional-N frequency synthesizers and frequency multiplication circuits used in millimeter-wave transceivers.

Francesco Tesolin received the M.S. and the Ph.D. degree (cum laude) in electrical engineering from the Politecnico di Milano, Milan, Italy, in 2019 and 2024, respectively, where he is currently working as a post-doctoral researcher.

His current research interests include design of digitally controlled oscillators (DCOs) and low-jitter digitally intensive fractional-N frequency synthesizers for communication systems and automotive radars. He was a co-recipient of the Jan Van Vessem Award for Outstanding European Paper of the 2023 International Solid State Circuits Conference.



Simone M. Dartizio was born in Milan, Italy, in 1995. He received the M.Sc. and Ph.D. degrees (cum laude) in electrical engineering from the Politecnico di Milano, Milan, Italy, in 2019 and 2023, respectively. From 2023, he has been a post-doctoral researcher with the Politecnico di Milano. His research interests include low-jitter frequency synthesis based on digitally intensive phase-locked loops and digital calibrations for mixed-signal integrated circuits. He was the recipient of the ISSCC 2023 Jan Van Vessem award for outstanding European paper and the 2023 SSCS Predoctoral Achievement award.



Salvatore Levantino received the Laurea degree (cum laude) and the Ph.D. degree in electrical engineering from the Politecnico di Milano, Milan, Italy, in 1998 and 2001, respectively. From 2000 to 2002, he was a consultant with Bell Labs, Lucent Technologies, Murray Hill, NJ, USA. Since 2005, he has been with the Politecnico di Milano, where he is currently a full professor of electrical engineering. He has co-authored over 180 scientific articles and the book "Integrated Frequency Synthesizers for Wireless Systems" (Cambridge University Press, 2007). He holds six patents. His research interests include wireless transceivers, frequency synthesizers, data converters, and power converters. He was a member of the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC), the Radio Frequency Integrated Circuits (RFIC) Symposium, and the European Solid-State Circuits Conference (ESSCIRC). He was a co-recipient of the ISSCC 2023 Jan Van Vessem award for outstanding European paper and the Best Paper Award of the 2018 International Symposium on Circuits and Systems (ISCAS). He was a Guest Editor for two issues of the *IEEE Journal of Solid-State Circuits* and an associate editor for the IEEE Transactions on Circuits and Systems—I: Regular Papers and the IEEE Transactions on Circuits and Systems—II: Express Briefs. He was an IEEE SSCS Distinguished Lecturer.