RF Technology Roadmap for 5G and 6G RF Front-end Systems

Yvan Morandini

Abstract—**The advent of 5G advanced and transition to 6G wireless systems are ushering in a new era of challenges for radio frequency (RF) front-end module design and integration. To seamlessly navigate this technological shift, which incorporates new sub-20-GHz spectrum (FR3) allocation and the expanded utilization of millimeter-wave frequencies (FR2), the foundational RF technology substrate must be engineered to meet the stringent performance demands of next-generation 5G advanced and 6G RF front-ends. This evolution requires cutting-edge semiconductor technologies to optimize signal integrity, power efficiency, and system integration. In our forthcoming discussion, we will present RF substrate technology roadmap, crucial for architecting the resilient, high-performance RF systems that will underpin the next-generation 5G and 6G wireless infrastructure.**

In this paper, we will provide a roadmap of RF technology including the engineered substrates enabling to solve design challenges of wireless communication systems.

Index Terms— **Engineered substrates, RF front-end, RF-SOI, FD-SOI, POI, GaN and InP**

I. INTRODUCTION

THIS paper describes recent developments of engineered substrate for next-generation cellular RF front-end (RFFE) design, addressing the evolving hardware requirements for future mobile devices. The first section discusses the evolution and challenges of 5G and upcoming 6G RFFEs. The following sections present key advancements in engineered substrates aimed at overcoming these challenges, including RF-SOI (Radio Frequency Silicon on Insulator), FD-SOI (Fully Depleted Silicon on Insulator), piezo on insulator (POI), GaN, and InP technologies.

This work is related to Move2THz, a project supported by the Chips Joint Undertaking (Chips JU) under grant agreement number 101139842. The Chips JU receives support from the European Union's Horizon Europe research and innovation program and the National Authorities.

Yvan Morandini (yvan.morandini@soitec.com) is with Soitec, France.

II. 5G AND NEXT GENERATION 6G RFFE EVOLUTION AND CHALLENGES

The key challenges and evolution of 5G RFFE are comprehensively detailed in [1]. The frequency bands for 5G new radio (5G NR) now include Wi-Fi bands at 2.4, 5.8, and 6 GHz. To support high data rates, the RFFE architecture has become increasingly complex, accommodating the coexistence of Wi-Fi and 5G, new frequency bands, and dual connectivity. Within the FR1 spectrum, new sub-6GHz bands have been introduced to address the data limitations of 4G. These bands, in conjunction with reframed 4G bands, require additional receive and transmit modules. In the FR2 spectrum, 5G millimeter-waves (mmWave) at 28 and 39 GHz offer significantly higher bandwidths compared to 4G, with bands extending to 52 and 71 GHz. The high frequency losses associated with these high frequency bands make it essential to integrate the antenna and RFFE into a

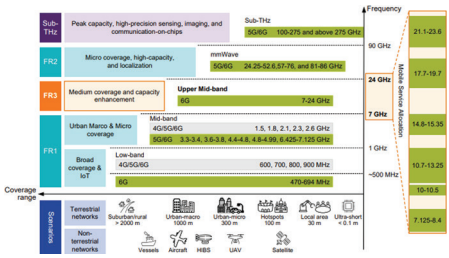

Fig. 1. Spectrum overview for mobile networks [2].

single module, referred to as antenna in package. Multiple antenna modules are required within devices to mitigate the effects of user hand interference. The 5G mobile architecture requires dual connectivity to utilize both 5G and LTE bands, as standardized in 3GPP Release 15, thereby improving coverage and data rates. To facilitate faster data transfer, 5G smartphones must support 4 × 4 MIMO for downlink and 2 × 2 MIMO for uplink. The increased complexity arising from coexistence of 4G and 5G, along with the introduction of new 5G bands, underscores the need for advanced RF front-end modules (FEMs).

Given the congestion in the sub-6G spectrum, the telecommunications industry is increasingly exploring higher frequencies to achieve greater bandwidth, which is essential for future 5G and 6G deployments. The newly allocated FR3 spectrum, ranging from 7 to 24 GHz (Figure 1), offers a promising solution by combining the broad area coverage characteristics of sub-6-GHz frequencies with the enhanced data rates and capacity typical to mmWave bands. FR3 provides distinct advantages over FR1 by offering wider channel bandwidths. Compared to FR2, FR3 experiences reduced signal attenuation and entails lower hardware implementation costs, making it a valuable option for next-generation networks.

To efficiently operate RFFEs within the 7–24 GHz range, novel transceivers and RFFEs must be designed. These components must incorporate up/down converters, ADCs (Analog to Digital Converter) with wider bandwidth considerations, and power amplifiers (PA) capable of linear output in FR3. Furthermore, existing transceiver architectures developed for FR1 and FR2 will need to be adopted for compatibility with FR3. FR3 represents an ideal band for hybrid beamforming architecture, balancing spatial multiplexing in FR1 while reducing beamformer complexity and power consumption in FR2. The central challenge lies in harmonizing optimization-based and learning-based designs for the hybrid transceiver architecture. As we advance this architecture, extending it toward RF-SOI technology will be essential for achieving optimal performance.

Utilizing the THz band presents significant challenges for transceiver hardware design [3]. Operating at such high frequencies imposes stringent requirements on semiconductor technology. Even with state-of-the-art technologies, the operating frequency may approach or even exceed the maximum frequency where the semiconductor can effectively provide power gain. This results in a severely degraded receiver noise figure and reduced transmitter efficiency compared to lower frequency operations. To maximize high-frequency gain, technology must employ scaled-down feature sizes, necessitating low supply voltages to maintain reliability. This reduction in supply voltage, however, diminishes the achievable transmitter output power. Additionally, the degraded receiver noise figure, reduced antenna aperture, and wide signal bandwidth at these high frequencies naturally leads to very short link distances.

The key challenges for this evolution are:

- Coexistence of 5G, 6G, and Wi-Fi bands: Increased interference risk due to overlapping frequency usage.

- New dedicated bands for 5G and 6G: More carrier aggregation will require additional filter paths, increasing the strain on the RF bill of materials footprint.
- Bandwidth requirements: Support for bandwidths up to 100 MHz.
- Higher power class devices: Devices requiring up to 26 dBm at the antenna, as defined by 3GPP. This new power class category establishes the maximum transmit power over the full 5G NR channel bandwidth, addressing the link budget limitation from user equipment to the base station. Higher transmit power from user equipment enables better cell coverage, necessitating more efficient high PAs.
- Improved PA efficiency: Specifically enhancing efficiency at higher frequencies.
- Technology scaling: Extend CMOS maximum frequency and III-V RF technology CMOS compatible.

III. NEXT-GENERATION RF-SOI TECHNOLOGIES

While RF CMOS SOI technologies are well-established for RF switches in FEMs, they have also been implemented for low-noise amplifiers (LNAs) by reducing gate length to improve gain and noise figures. The integration of more FEM functions into a single chip becomes increasingly crucial in the FR2 mmWave and FR3 ranges to minimize package-related losses. Addressing this integration challenge requires continuous improvement in figures of merit such as f_t (cutoff frequency) and f_{max} (maximum oscillation frequency).

RF-SOI technology, depending on the application and frequency bands, can be compatible with CMOS technology down to 40 nm, as illustrated in Figure 2. Next-generation RF-SOI technologies will require to develop new RFeSI™ trap-rich technology, maintain good linearity performance, and be compatible with 40 nm CMOS technologies. Next-generation mmWave trap-rich substrate solutions will enable a lower second harmonic performance of 50 dBm while being compatible with stringent overlay performance requirements as depicted in Figure 3.

Application	Frequency band	Range (coverage)	RF-SOI Technology platform			
			180nm	130/90nm	65/55nm	45/40nm
Antenna tuners	sub-6GHz		✓	✓	✓	
	6 - 15GHz			✓	✓	
	mmWave					
Switch	sub-6GHz	short	✓	✓	✓	✓
		wide	✓	✓	✓	
	6 - 15GHz			✓	✓	✓
	mmWave				✓	✓
LNA	sub-6GHz	short	✓	✓	✓	✓
		wide			✓	✓
	6-15GHz			✓	✓	✓
	mmWave				✓	✓
mmW standalone* RFFE	mmWave				✓	✓
						✓

Fig. 2. Applicability of RF-SOI technology platforms.

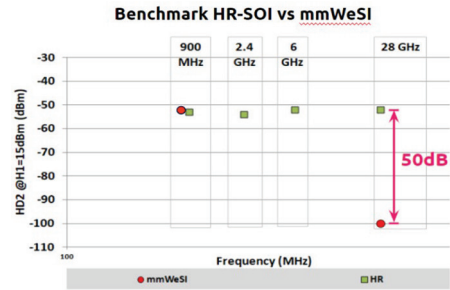

Fig. 3. Second harmonic as function of the frequency comparing HR-SOI with mmWave trap-rich RF-SOI. Input power: 15 dBm.

IV. NEXT-GENERATION FD-SOI TECHNOLOGIES

The use of a commercial low-leakage FD-SOI RF planar CMOS platform has successfully demonstrated the advantages of this mmWave RFFE architecture in the mobile market. Compared to CMOS bulk technology [4], it improves PA efficiency, enhances the noise figure of LNAs, and optimizes power consumption. The evolution of 5G advanced and 5G systems will require extending the maximum

frequency of CMOS FD-SOI technology up to 500 GHz and looking into the integration of high resistivity option. Today, the 22 nm FD-SOI technology has demonstrated f_t/f_{max} of 370 GHz/410 GHz.

A promising solution to extend RF performance while enabling digital scaling is the use of strained layers. The Smartcut technique can be employed to transfer bi-axially strained silicon films, grown on fully relaxed SiGe buffer layers on Si bulk donor wafers, to create unique strained SOI. This approach leverages the carrier mobility enhancement offered by tensile-strained silicon [5,6].

The high resistivity substrate option is a significant enhancement to achieving ultimate mmWave performance. The engineering challenges associated with this new wafer generation are detailed in the study [7]. Among the various options for highly resistive silicon, low and high interstitial oxygen (Oi) materials are mostly used to achieve the desired resistivity performance on SOI handles. However, these materials are less compatible with FD-SOI technology, as they can be highly sensitive to slip-line issues or wafer deformation, it could lead to overlay errors. Additionally, high Oi substrates may encounter inspectability and co-integration issues due to the presence of crystal originated particles. Soitec has developed a specific process to tackle these challenges. They demonstrated how substrates were specifically engineered to achieve the appropriate resistivity targets around 1000 Ω.cm, ensuring stability at depth through various additional anneals and maintaining compatibility with customer processes. This process also ensures excellent mechanical performance, minimizing slip-line generation during fabrication processes, and avoiding overlay issues typically associated with slip-lines or excessive presence of bulk micro defects at depth, which can cause dislocations and plastic deformation. Furthermore, [8] describes that the combination of high resistivity substrate with PN interface passivation technique is particularly relevant for FD-SOI. By utilizing alternating regions of P- and N-type doping, the conductive interface is locally interrupted by induced depletion junctions. This chain-series combination significantly increases the overall substrate impedance (ρeff).

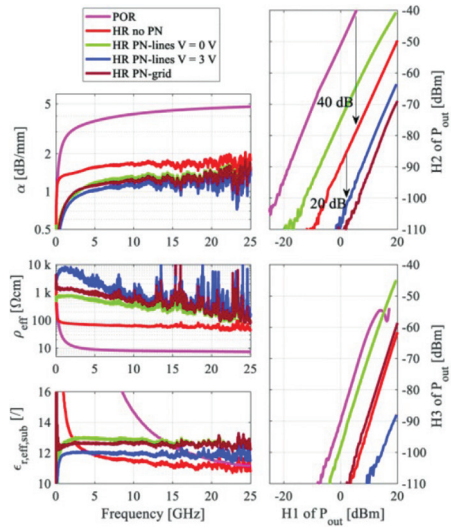

Fig. 4. RF substrate figures of merit were measured from M1M2 CPW lines. Small-signal data, including α (attenuation constant), ρeff (effective resistivity), and εr_{effsub} (effective relative permittivity of the substrate), were extracted using multiline thru-reflect-line calibration from multiple CPWs. Large-signal data, including harmonics H1, H2, and H3, were measured at a 900 MHz fundamental frequency on a 2-mm-long CPW [8].

Measurements of coplanar waveguides have demonstrated significant improvements in harmonic performance, as illustrated in Figure 4.

V. PIEZO MATERIAL FOR RF FILTER

The adoption of massive input massive output (MIMO) in receiver and

	SAW	TC-SAW	BAW	SAW on POI
Operating Frequency (GHz)	Low - High	Low – High	High Ultra High	Low - High Ultra High
Quality Factor (Bode Q) @2GHz	1500	<1500	4000 (AlN)	>4000
Coupling factor k^2	<7% ($LiTaO_3$)	<7%-$LiTaO_3$ <20% -$LiNbO_3$	<7% - AlN <12% - AlNSc	>8% - $LiTaO_3$ >20% -$LiNbO_3$
Temperature Compensation (ppm.K^{-1})	>40 - $LiTaO_3$	<20 - $LiTaO_3$	>20	< 10 - $LiTaO_3$
Substrate complexity	Low	Low	Low	High
Process complexity	Low	Mid	High	Low
Integration	Low	Low	Low	High

Fig. 5. Piezo on insulator (POI) versus alternative RF filter technologies benchmarking.

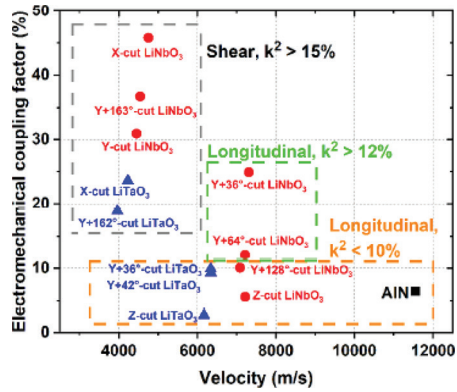

Fig. 6. Electromechanical coupling factors and bulk wave velocities for various $LiNbO_3$ and $LiTaO_3$ commercial cuts [9].

transmitter front-ends, combined with the increase in the number of bands, carrier combinations, and signal paths, significantly raises the demand for RF filtering elements in the RFFE. POI substrates present a promising solution to accommodate this growing demand within the same or even smaller footprint. These substrates provide stable high rejection and low loss even at high temperatures, and they simplify the manufacturing process.

Figure 5 illustrates the advantages of using POI substrates by comparing competitive technologies over different frequency bands.

In single crystal materials like $LiNbO_3$ and $LiTaO_3$, the polarization and velocity of acoustic waves can be adjusted by choosing the appropriate crystal orientation. These materials enable electromechanical coupling factors up to 45% and acoustic velocities between 3960 and 7320 m/s, which is depicted in Figure 6. This versatility makes them suitable for high-frequency applications.

The use of $LiTaO_3$ has been demonstrated for POI technology and preliminary studies are extending the use of $LiNbO_3$ beyond 3.5 GHz. Soitec and partners are investing $LiNbO_3$ as a good alternative to extend POI technology beyond 3.5 GHz and to extend the bandwidth of RF filter below 3.5 GHz.

VI. RF GAN TECHNOLOGY

RF GaN technology has shown significant advantages for RF PAs in 5G base stations, primarily utilizing GaN on SiC substrates. However, as massive MIMO infrastructure and beamforming transmission are deployed, the output power handled by individual PAs significantly decreases, despite a corresponding increase in the number of PA devices. Moreover, the adoption of the FR3 band for mobile user equipment could potentially disrupt the PA technology. Addressing the new device requirements will necessitate specific advancements in epitaxial GaN development [10] through:

- Reduction of conducting RF losses: Minimizing RF losses at the GaN/Si interface up to mmWave frequencies is crucial for optimal performance.
- Engineering low-trapping (Al,Ga)N buffer stacks: This involves incorporating carbon into resistive layers and back-barriers to enhance electron confinement and reduce trapping effects.

- Barrier design: Careful design of the barrier layer is necessary to ensure efficient electron mobility and overall device performance.
- Capping or passivation layer: Special attention is required for the capping or passivation layer, particularly when using MOCVD-grown SiN, to protect the device and maintain its electrical properties.

The study [11] describes the suitability capability of RF GaN for mobile user equipment design and highlighted advancements in epitaxial layer stack development. To meet voltage requirements, GaN device development incorporates a new epilayer featuring in undoped AlInN barrier layer, undoped GaN buffer layer, and an AlGaN back barrier on Si substrates. Devices using this structure exhibit exceptional performance across a voltage range from 1.5 to 12 V, achieving power density (Pd) values of 2.66 and 4.23 W/mm at Vds of 8 and 12 V, respectively, with power added efficiency (PAE) exceeding 60%.

Soitec [12] developed a pioneering concept with Smart Cut™ technology, introducing GaN-on-X substrates that overcome the physical limitations of heteroepitaxial growth. This method involves transferring a thin GaN film onto a handling substrate (such as Si, SOI, polySiC, etc.), tailored specifically for RF applications. This innovation enables the creation of devices with superior thermal resistance (Rth), higher power density, improved power efficiency, and reduced memory effects, enhancing linearity.

VII. INDIUM PHOSPHIDE (INP)

The sub-THz spectrum (FR4) including frequencies beyond 100 GHz, such as the D-band, gained significant interest for achieving the ultra-high data rate goals of next-generation 6G cellular networks. However, operating at carrier frequencies above 100 GHz presents substantial challenge, particularly in terms of power efficiency. To address these challenges, semiconductor and compound technologies with transistor f_{max} values exceeding 500 GHz may be necessary to enhance efficiency, gain, and noise performance. While SiGe technology holds the potential for improving silicon transistor performance, current advancements in InP technology offer the best front-end performance at sub-THz frequencies. This technology provides superior PA P_{out} and PAE as well as a low noise figure characteristics.

Despite its advantages, InP technology is limitedly used in markets with low volume production. That is mainly related to its manufacturing constraints, such as their small wafer diameters and high costs. To thrive in the consumer market, InP needs reliable and cost-effective manufacturing processes. An innovative method for producing large-diameter (up to 300 mm), cost-effective InP wafers is detailed in [10]. This method is based on wafer reconstruction and reclaiming. Building upon the foundational aspects of the SmartCut™ technology and the tiling approach, the process begins by selecting smaller diameter III-V wafers, such as those made from GaAs or InP. These are traditionally limited to 100 or 150 mm due to the constraints in bulk material production. These smaller wafers are then meticulously arranged and bonded onto a larger, 200 mm silicon wafer, creating a composite or pseudo-donor wafer. This approach not only circumvents the diameter limitations of traditional III-V substrates but also leverages the robustness and scalability of silicon infrastructure.

REFERENCES

[1] Y. Morandini, “RF technology roadmap for 5G and 6G RF front end systems”, ESSDERC 2023.

[2] Z. Cui,“6G Wireless Communications in 7-24 GHz Band: Opportunities, Techniques, and Challenges”, IEEE System and control 2024

[3] H. Tataria “6G Wireless Systems: Vision, Requirements, Challenges, Insights, and Opportunities”, Proceedings of the IEEE Volume: 109, Issue: 7, July 2021

[4] V. Bhagavatula et al., “A 5G FR2 Power-Amplifier With an Integrated Power-Detector for Closed-Loop EIRP Control,” in IEEE Journal of Solid-State Circuits, vol. 57, no. 5, pp. 1257–1266, May 2022.

[5] C. Sun et al, “Enabling UTBB Strained SOI Platform for Co-integration of Logic and RF: Implant-Induced Strain Relaxation and Comb-like Device Architecture”, VLSI 2020

[6] B. De Salvo et al, “A mobility enhancement strategy for sub 14nm power-efficient FDSOI technologies” IEDM 2014

[7] I. Bertrand, “Development of High Resistivity FD-SOI Substrates for mmWave Applications”, ECS Transactions, Volume 108, Number 5, 2022

[8] M. Rack et al., “High-Resistivity Substrates with PN Interface Passivation in 22 nm FD-SOI”, VLSI 2022

[9] M. Bousquet et al., “4.2 GHz LiNbO3 Film Bulk Acoustic Resonator,”

[10] 2021 IEEE International Ultrasonics Symposium

[11] M. Germain et al. “GaN epitaxial solutions for RF and Power devices”

[12] K. Takeuchi et al., “Low-Voltage Operation AlInN/GaN HEMTs on Si with High Output Power at sub-6 GHz”, IMS June 2023

[13] G.Gaudin, ICNS 14, 14th International Conference on Nitride Semiconductors, 2023, Fukuoka, Japan, ThP-GR-LN4

[14] B. Ghyselen et al., “Large-Diameter III–V on Si Substrates by the Smart Cut Process: The 200 mm InP Film on Si Substrate Example,” Phys. Status Solidi A, Vol. 219, Issue 4, Feb. 2022.

Yvan Morandini received the MSc degree in engineering from Grenoble Alpes University, France, in electronics and radiofrequencies in 2005 and the Ph.D. degree from Lille University in 2008. After three years in STMicroelectronics, he then moved to IBM, Dolphin Integration and then to SOITEC. He is currently Strategic Marketing Senior Manager at SOITEC. He has 20 years of experience in the semiconductor industry including characterization, modeling, and design. He has authored/co-authored over 15 papers in international, peer-reviewed journals and conferences, and is a Member of Institute of Electrical and Electronics Engineers (IEEE).