Challenges for 2.5D and 3D Integration of InP HBT Technology

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Abstract—**Indium phosphide (InP) double heterojunction bipolar transistor (D-HBT) technology can be co-integrated with silicon (e.g., silicon-on-insulator (SOI), fully depleted SOI (FDSOI), silicon germanium bipolar complementary metal-oxyde semiconductor (SiGe BiCMOS)) and antennas in order to benefit from their superior high-frequency performances in a cost-effective manner (using 2.5D, 3D integration techniques), while benefiting from the higher integration level provided by silicon ICs. This paper presents the strategic and practical InP D-HBT technology development challenges for the successful 2.5D/3D integration of millimeter wave and sub-THz applications from the perspective of InP manufacturing.**

Index Terms—**Double heterojunction bipolar transistor (D-HBT), indium phosphide, InP/InGaAs, modeling, terahertz (THz), 2.5D, 3D integration.**

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I. INTRODUCTION

In order to transfer the ever-increasing amount of data stored and processed in the digital world from one point to another, analogue transmission channels are unavoidable and are becoming today (ironically) the real bottleneck of our information society. Future 6G communications, Cloud computing and Artificial Intelligence (AI) altogether, to cite only a few applications, are expected to consume more transmission capacity (see Figure 1) than what can be provided by the optical fiber and wireless communications systems' projected capacity scaling. In order to anticipate this huge demand of bandwidth and higher operating frequencies (and consequently the need for very high-speed electronics), researchers have been intensively developing high-speed silicon technologies. It is well known that the maximum oscillation frequency (f_{MAX}) of silicon CMOS (and its various silicon-on-insulator (SOI) and fin field-effect transistors (FinFET) variants) does not improve anymore with gate length reduction since the 28 nm node [1] [2], and is consequently not the technology of choice for future millimeter wave (mmWave) and sub-THz transceiver front-end, despite their superior integration level capabilities and lower cost. As an alternative, SiGe BiCMOS technologies have experienced a remarkable

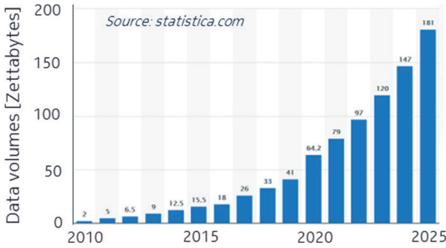

Fig. 1. Volume of data/information created, captured, copied, and consumed worldwide.

performance increase over the last two decades [3][4], making them the technology of choice for radio frequency (RF) front-ends, whenever pure CMOS technologies cannot meet the specifications (e.g., for high-frequency (HF) operation). Nevertheless, for next-generation communication and sensing applications targeting the 100–300 GHz bands, for which the use of antenna arrays and beam steering is necessary to compensate for atmospheric attenuation, the limits of SiGe BiCMOS technology are perceived. Actually, power consumption is a critical metric for large power amplifier (PA) – antenna arrays, making the power added efficiency (PAE) specifications of the PA out of reach of present SiGe BiCMOS processes. Therefore, more exotic technologies, such as indium phosphide (InP) heterojunction bipolar transistor (HBT) technologies, are presently considered as a potential contender. Interestingly, research is gaining traction in this area lately, and literature dealing with CMOS or SiGe BiCMOS hetero-integration (or 2.5D/3D packaging) with InP is flourishing. Indeed, from a pure material performance point of view, there is no debate that InP is superior to silicon in terms of speed, but significant challenges have to be overcome to make it a viable option for future mmWave and sub-THz applications. This paper presents these challenges from a technical, practical, and economical perspective. Section II will present the state-of-the-art and will emphasize InP HBT performance advantages over other high-speed technologies. Section III will detail the challenges for InP high-volume manufacturing, while Section IV will present the challenges related to 2.5D/3D integration. Section V will introduce the requirements regarding advanced compact modeling of InP HBTs, and finally a conclusion will be drawn in Section VI.

II. TECHNOLOGY STATE-OF-THE-ART AND COMPARISON

Figure 2 presents a summarized state-of-the-art of semiconductor technologies suitable for mmWave and sub-THz applications (gallium nitride (GaN) technologies are intentionally not shown as they are commonly considered as more suitable for applications below e.g. 100 GHz and higher power). Figure 2 presents the geometrical mean of f_T and f_{MAX} on the y-axis (as this figure of merit (FoM) is a balanced indicator of transistor's high frequency performance) versus breakdown voltage (or supply voltage for CMOS). As it can be observed, the various technology trends follow roughly the "pseudo" Johnson limit (we use the term "pseudo" here, as the standard Johnson limit refers to f_T only): the higher the transistor speed is, the lower is its voltage drive capability. Note that some moderate deviations from the hyperbolic trend are noticeable in Figure 2, which is due to the positive impact of smaller lithography on f_{MAX} via external parasitic reduction. This, however, does not dramatically change the conclusions that can be drawn from this graph. When looking only at the y-axis, we can note first that the CMOS limitations mentioned in the introduction are clearly visible. Also, it is observed that the most advanced SiGe HBTs (with f_{MAX} > 600 GHz, e.g., [3]) are able to catch up with a majority of the InP HBT technologies. This observation is certainly one of

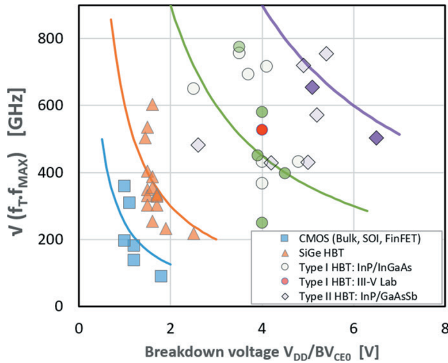

Fig. 2. Geometrical mean of f_T times f_{MAX} versus breakdown voltage. Filled markers represent technologies with known monolithic microwave integrated circuit (MMIC) fabrication capabilities, and empty markers represent technologies able to demonstrate transistors only (no known published circuit results).

the reasons why some "silicon exclusive advocates" argue that InP is not needed in the semiconductor ecosystem apart for some extremely reduced niche markets (astronomy observation, high-end characterization equipment, etc.).

This assertion needs to be reconsidered somehow, when considering the *x*-axis (breakdown voltage): while SiGe HBTs can almost play on par with InP HBTs in case of small signal operation, this is a misleading conclusion when considering large signal operation (PAs, for instance, which are a key element of future 6G transmission systems).

Actually, the breakdown voltage of Type I HBTs is more than two times larger than that of SiGe HBTs, and the difference is even more pronounced for Type II HBTs which exhibit impressive $\sqrt{(f_T \cdot f_{MAX})} \cdot BV_{CEO}$ product > 3600 GHz.V [5][6][7]. This brings a significant advantage in terms of power drive capability (P_{SAT}) and in terms of PAE for mmWave PA design (noting that the device efficiency is proportional to $1-V_{knee}/V_{BV}$, where V_{knee} is the knee voltage and V_{BV} is the breakdown voltage of the device).

Another important information that can be extrapolated from Figure 2 is the perspective of future improvements. Considering that independently of the technology, optimizing the transistor for higher speed (i.e. higher f_T and f_{MAX}) results in trading off the breakdown voltage (i.e., moving along the hyperbola imposed by Johnson limit), InP HBTs have much more room for improvement. Indeed, going "beyond" the Johnson limit for a given material system requires major structural or technological modifications, which usually come at the expense of process complexity or other performance penalties. To summarize, not only InP HBT technologies currently have a performance advantage (especially when considering PAs above 100 GHz), but they also have the highest potential for (straight forward) improvement in the future.

III. CHALLENGES TOWARDS HIGH VOLUME INP HBT MANUFACTURING

Although InP HBT technologies offer unparalleled performance advantages, its market adoption has been limited to only a few application areas and very limited volume due to some major manufacturing limitations with respect to silicon: higher process cost, lower manufacturability, material brittleness and scarcity, smaller wafer size, and incompatible back-end with mainstream silicon packaging solutions.

A. Fabrication Cost and Other Considerations

InP HBT processes are typically limited to small diameter wafers: many academic labs still use 2″ wafers, while industrial labs and foundries are typically relying on 3″, 4″, or (rarely) 6″ wafers. This is an obvious limitation to move to

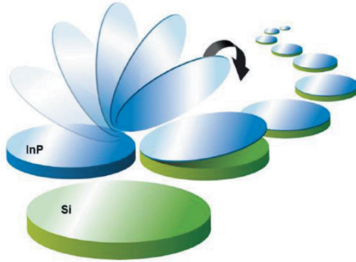

Fig. 3. InPoSi wafer fabrication principle (SOITEC SMARCUT™ process).

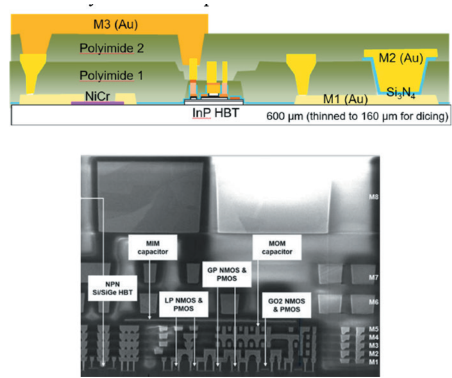

Fig. 4. BEOL of line of the InP HBT technology from III-V Lab (top, not to scale) and BiCMOS55 from ST microelectronics [9] (bottom).

high-volume manufacturing and to benefit from the economy of scale prevailing in the silicon world. Therefore, research is ongoing to develop InP HBT processes on InPoSi (InP on silicon) wafers (e.g., MOVE2THZ project [8]). InPoSi is a fabrication process consisting in bonding a thin slice of InP from an InP donor wafer on a silicon wafer (see Figure 3). The donor wafer can be reclaimed several times (which is a mitigation to indium material scarcity) and the resulting InPoSi wafer is therefore mechanically more robust, thus improving manufacturability. Moreover, InPoSi can be used to produce 8″ or 12″ wafers through "wafer tiling," thus solving the (donor) wafer size issue mentioned earlier and reducing raw InP wafer cost. Despite this improvement on raw material, the initial epitaxy step still constitutes a major cost contributor that cannot be fully mitigated by the wafer size increase. Therefore, in order to circumvent this problem, alternative paths for cost reduction need to be employed.

B. Alternative Strategies Towards High-Volume Manufacturing

One of the simplest options for reducing InP die cost is to reduce the chip footprint (i.e., minimizing the cost for a given functionality). The solution to this problem is not obvious because analogue and RF functions do not scale in a straightforward manner (as opposed to digital functions that scale quadratically with technology minimum feature size).

Typical InP HBT technologies have 2–4 relatively thin metal layers. More advanced back-end of lines (BEOLs; i.e., more metal layers, thicker metals, and inter-metal dielectric layers) can significantly reduce both dielectric losses at mmWave and/or the on-chip matching networks' footprint and power combining stages (see Figure 4 for an example of comparison of a typical SiGe BiCMOS [9] and of a typical InP HBT BEOL [10]). Although most of the (dense routing) lower metal layers of silicon technologies may be of little use in an optimal InP HBT process, the top thicker metal layers could be advantageously used for mmWave interconnections. In parallel, development work for higher density routing also needs to be conducted, as most InP HBT manufacturers sometimes use (unnecessary) conservative design rules (lift-off techniques are widely used in InP HBT processes, which partly explain these stringent design rules, but part of the layout restrictions simply come from more simplistic design rules implementation in computer-aided design (CAD) verification

tools). Another issue limiting die size reduction is the integrated capacitors and resistors that consume a lot of space on the chip. Compared to the wide variety of integrated RF resistors available in silicon technologies (ranging from a few Ω/□ to several kΩ/□) and double density integrated MiM capacitors (typically from 2 to 4 fF/µm²), the typical single NiCr resistor layers (~50 Ω/□) and Si_3N_4 MiM capacitors (typically below 0.5 fF/µm²) available in typical InP HBT technologies are another limiting factor. Finally, through substrate vias (TSVs) typically used to improve the IC HF stability and eliminate parasitic substrate modes, when available in a given process, consume a large footprint: finding alternatives (such as the use of thin film microstrip lines (TFMSLs)) would be beneficial for the overall die size reduction.

Ultimately, InP area reduction could be pushed even further by reducing the InP die size to the transistor area and its connections pads [11]. This is one of the possible options allowed by co-integration: reducing the die size to its minimal requirement, that is, down to a single transistor. One option is to replace an MMIC (e.g., a Power Amplifier (PA) or Low Noise Amplifier (LNA), including its connections, matching and stabilization input and output networks, decoupling capacitances and its biasing transmission lines and resistors) by a single multi-finger transistor. Considering the example of the PA design shown in Figure 5 (left), whose size is 1.2 × 1.5 mm² and a typical InP HBT structure of 260 × 160 µm² shown in Figure 5 (right), the area reduction ratio can be as high as 40 (and so the cost of the InP die in the bill of material). This option implies other challenges that still need to be solved: all the removed functions need to be efficiently realized in CMOS or SiGe BiCMOS and connected via low loss interconnections. Moreover, in order

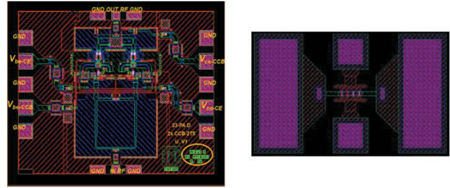

Fig. 5. PA MMIC chip design 1.2 × 1.5 mm² (III-V Lab) (left), multi-finger transistor structures in its RF pads 260 × 160 µm² (right).

to efficiently co-design the silicon chip with the InP HBT transistor, significant effort has to be made in the compact modeling of InP HBTs and in the electrical–electromagnetic co-simulation of the whole system in a complex multi-material environment.

IV. CHALLENGES RELATED TO 2.5D/3D INTEGRATION

A. *Generic Requirement for Hetero-integration*

Describing all possible 2.5D/3D hetero-integration schemes of InP HBT technology with silicon dies is beyond the scope of this paper; it is still interesting to review the requirements on the InP technology side in terms of BEOL. Figure 6 shows some possibilities for SiGe/CMOS co-integration with InP. While SiGe die flip chipping is widely used, flip chipping InP dies is not straightforward, especially for PAs due to thermal constraints. The gold back-end and lack of top passivation (making InP BEOL incompatible with copper pillars), heat dissipation, and HF de-tuning are among the difficulties to overcome. Regarding thermal aspects, the use of InPoSi wafers is still unclear and will remain unclear until the first HBTs become available on InPoSi (while silicon thermal conductivity is better than InP, thermal barriers between InP and Si can mitigate thermal dissipation gains.

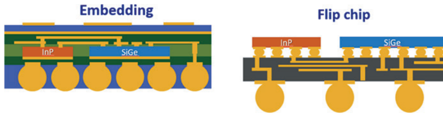

Fig. 6. 2.5D/3D integration schemes examples (SiGe in blue and InP in brown).

Moreover, significant work has to be done on the back-end to (i) make it compatible with mainstream flip-chip techniques (finishing/passivation) and (ii) make the die more immune to de-tuning. For this, the InP chip BEOL should have an optimized back-end (more metal layers and thicker metals) to allow low-loss TFMSLs with potentially top and bottom ground planes in order to confine the electromagnetic (EM) field within the back-end. The ultimate goal in this matter is to bring InP dies close to the "chiplet" concept.

Embedding (see Figure 6) is the solution that has been chosen within the SHIFT project [12] for InP/BiCMOS co-integration demonstration. This solution in [13] allows an interesting design option to co-integrate the SiGe BiCMOS chip, the InP PA, and the antenna in order to demonstrate beam-steering capabilities. Demonstration of this principle is currently ongoing as part of the SHIFT project activities. The challenges on InP technologies are the compatibility of BEOL with laser vias (metal thickness), BEOL finishing, and lack of backside metallization and TSV for the considered InP HBT technology (for heat dissipation).

B. Specific Technology Requirements for mmWave Applications and Hetero-integration with Silicon

Many InP HBT processes include TSV and backside metallization, which is currently not the case for III-V Lab's InP D-HBT technology. The III-V Lab technology [14] is natively optimized for high-speed analogue–digital electro-optical interfaces (for optical fiber applications): transistor's figures of merit are tuned for fast current switching, high voltage drive, wide band operation, and low process steps count. Due to the fast switching nature of the main application of this technology, TSV and backside metallization are therefore not considered as essential, taking into account the added process complexity and fabrication time. As shown in Section III.C, TSVs are also questionable regarding chip space requirements. TSV and backside metallization are required for mostly two aspects: (i) microstrip lines design and (ii) parasitic modes suppression. Regarding (i), as application frequency increases, the feasibility of microstrip lines becomes more and more difficult, since the substrate needs to be thinned to, e.g., values below 100 or even 50 μm to remain within the useful line impedance range, thus making the chips very fragile and degrading the process manufacturability. With this respect, switching to an alternative, such as TFMSL, is certainly desirable.

Regarding (ii), let us consider an example of parasitic mode excitation in a test structure based on coplanar wave transmission lines (see EM simulations results at 149 GHz shown in Figure 7, corresponding to a transmission dip of about

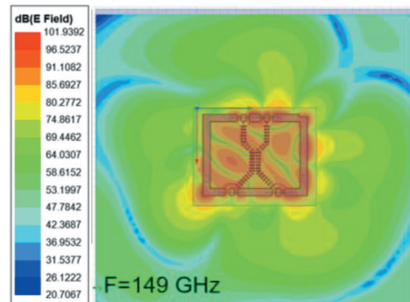

Fig. 7. EM simulation of a differential thru in coplanar wave transmission lines (corresponding to a circuit access). Excited parasitic modes are visible at 149 GHz.

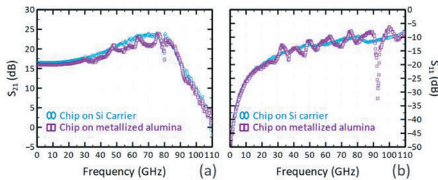

Fig. 8. Measured S parameters of an InP D-HBT AMUX-driver IC. S_{11} (left) and S_{21} (right) versus frequency, IC on a metallized ceramic carrier (red), and IC on a silicon carrier (blue).

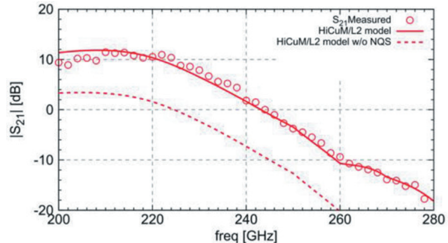

Fig. 9. Measurements/simulation comparison of the S_{21} parameter for a 220 GHz SiGe BiCMOS integrated LNA. Difference between simulations using HiCuM/L2 model with (solid line) and without (broken line) NQS effects.

8 dB). These parasitic modes' excitations are very detrimental for PA and LNA performances in, e.g., D- and G-bands, as they create dips and resonances in the IC response (to a certain extent, this is less detrimental for fast-switching digital circuits). Figure 8 shows an example of S-parameter measurements of an AMUX-driver IC [15] on both a gold-plated ceramic carrier and a silicon carrier. Indeed, parasitic modes excitation is strongly reduced on silicon, suggesting that the lossy silicon acts as an absorber. Therefore, future InP HBT technologies on InPoSi substrate may be less sensitive to parasitic modes excitations, which would remove the need for TSVs.

V. COMPACT MODELING CHALLENGES

Compact (SPICE-like) modeling of InP HBT technologies definitely lacks beyond silicon. Historically, due to missing suitable compact models for III-V HBTs, the III-V community mostly relied on hand-crafted and/or hand-customized models using either behavioral sources or symbolically defined languages. These models, although sometimes fairly elaborate and accurate for a specific application and/or bias and temperature range of operation [9], usually do not satisfy a wide variety of design needs, like e.g., BiCMOS models and process design kits (PDKs) do. Physics-based, scalable, statistical, and predictive models [14][16][17] are highly desirable to provide designers with larger search space and flexibility in their design points explorations, especially for mmWave and sub-THz applications where each and every dB of gain matters. Moreover, standardized models such as HiCuM/L2 [18][19] are available on virtually every CAD proprietary or open-source software as their Verilog-A code is available to users. An illustration of the need for advanced physics-based compact models such as HiCuM is the often underestimated effect for, e.g., 140–300 GHz frequency range, of non-quasi static (NQS) effects on HF linear gain prediction [20]. As depicted in Figure 9, neglecting NQS effects (which become significant when the application frequency approaches approximately $f_T/3$) can lead to severe discrepancies in the prediction of linear gain in amplifying stages.

VI. CONCLUSION

Today, InP HBT technology is confined to niche markets, thus limiting investment towards high-volume manufacturing and in turn limiting the usage of the technology for medium- to large-scale markets. This cycle can be broken with strategic investments in the InP ecosystem,

consisting only in fraction of what is necessary for silicon process developments. While InP HBT will remain a low integration level technology, it can definitely benefit to demanding mmWave applications as a complementary toolset of well-established silicon technologies via hetero-integration, as well as for >Tb/s optical communications. InP HBT cannot and will not replace SiGe BiCMOS, but can adequately complement their already powerful capabilities, provided adequate and ambitious (yet not out of reach) developments are achieved.

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