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Presentation title: RF-Heterointegration at Wafer-level and Panel-level for mmWave Applications

SHORT ABSTRACT OF PRESENTATION

Above 100 GHz packaging for millimeter-wave (mmWave) radars and phased arrays presents four fundamental packaging challenges:

- Reduction of antenna array pitch (e.g. 1 mm at 150 GHz), which requires the dense placement of antenna elements and electronics
- Increase in the size and types of chips needed: CMOS (beamforming) needs to be complemented with III-V (GaN, InP, GaAs) for final high-power low-noise stage
- Increase in metal and dielectric losses with frequency
- Thermal management as higher DC losses are generated in smaller areas leading to higher thermal densities

The packaging activities in imec's advanced-RF department aim to address these challenges and consist of two tracks.

The first track is a wafer-level packaging RF-interposer technology developed on 300 mm silicon substrates. This technology uses standard resistivity silicon substrates to reduce costs while achieving excellent mmWave and mixed-signal performance as the silicon substrate is shielded from the RF signals by using a ground plane. The main features of this technology are as follows:

- First, we incorporate a standard Cu damascene multi-layer backend process for digital interconnects for providing multiple parallel digital links in the low GHz range (1–3 GHz) but with high density (1um trace/space).
- Second, on top of the Cu damascene, we spin-coat two low RF-loss thick layers of polymer and semi-additive thick Cu Redistribution Layer (RDL)

layers. This provides an impedance matched mmWave link, which can provide broadband mmWave performance (DC – 200 GHz) at moderate densities (5 um trace/space, 30 um pitch).

- Third, high aspect ratio Through Silicon Via (TSV) (10:1), wafer thinning down to 50–100 um and TSV transitions through the silicon substrate to transfer mmWave signals to the backside of the interposer for 3D stacking and mounting.
- Fourth, we have also incorporated high performance and small footprint passives (MIMCAP up to 50 fF/um^2, high Q inductors, and TaN resistors) in the Cu damascene backend for supply decoupling at mmWave frequencies for GaN/InP/GaAs chiplets to be mounted on the interposer.
- Fifth, we have also demonstrated flip-chip interconnects for both CMOS (Cu backend) and III-V (GaN/InP/GaAs with Au backend) chiplets on our interposer with 40 um micro-bump pitch with broadband RF performance up to 110 GHz (to be extended further in frequency). Demonstrators for phased arrays and radars using this technology are being developed at imec-Florida, USA under a US National Science Foundation Engines grant.

The second track on panel-level packaging focuses on two activities:

- First, die embedding of mmWave chipsets in an organic core package and development of antenna-in-package technology. Die-embedding offers two benefits over flip-chip interconnect: (1) the connections to the antenna are shorter as the mmWave signal needs to traverse only the top half of the build-up and (2) the bottom half of the build-up can be used for thermal management.
- The second activity involves the development of air-filled substrate integrated waveguide (AFSIW) technology for mmWave applications where we have demonstrated an AFSIW with loss of 0.07 dB/mm at 140 GHz with solid sidewalls and broadband launcher with insertion loss of 1.1 dB.

Both activities are being continued further with partners of the advanced-RF program.

KEYWORDS

RF, heterointegration, CMOS, III-V, antenna, phased array, InP, GaN, GaAs, interposer, chiplet, TSV, flip-chip, die embedding, air-filled substrate integrated waveguide (AFSIW).

BIOGRAPHY

Siddhartha Sinha has been a part of the advanced-RF department of imec, Leuven, Belgium, since 2015. He is responsible for electromagnetic modeling, III-V/CMOS heterointegration, mmWave antennas, packaging and system technology co-optimization (STCO) of mmWave systems. Between 2010 and 2015, he was a scientist with the Ferdinand-Braun-Institut (FBH), Berlin, Germany, working on mmWave interconnects and equivalent circuit modeling for FBH's InP transistor technology. Between 2004 and 2006, he was a scientist at Defence R&D Organisation (DRDO), Bangalore, India, working on travelling wave tubes. He holds a bachelor's degree from Visweswaraya Technological University, India and a master's degree from Technical University Munich, Germany.