Analog Multiplexing for Bandwidth and Sampling Rate Multiplication of Digital–Analog Converters in Coherent Optical Transmission Systems

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Abstract—**This paper presents the concept of analog time-division multiplexing of DAC output signals and introduces a frequency-domain explanatory model for both 2:1 and 4:1 analog multiplexer (AMUX) variants. Also, it presents 2:1 and 4:1 AMUX circuit concepts and related design considerations along with measurement and simulation results of a 2:1 AMUX module, realized in SiGe BiCMOS technology exhibiting an effective resolution of over 7 bit and a maximum sampling rate of 186 GS/s.**

Index Terms—**Analog multiplexer, AMUX, ENoB, SiGe-BiCMOS, DAC, high speed, 4:1 AMUX**

I. INTRODUCTION

COHERENT optical transmission systems are pivotal for transporting aggregated data traffic in metro, long-haul, and submarine domains. These systems achieve significantly higher transmission rates compared to other parts of the communication network, primarily due to their utilization of extremely high transmission bandwidths combined with high spectral efficiencies. Currently, systems with approximately 130 GHz bandwidth are being introduced to the market [1], supporting bit rates of up to 1.2 Tb/s for long-haul transport and 800 Gb/s as pluggables for metro transport. Such high transmission bandwidths necessitate analog interfaces with electrical bandwidths exceeding 65 GHz. On the transmitter side, these analog interfaces comprise digital-to-analog converters (DACs), driver amplifiers, and modulators, while on the receiver side, they include photodiodes, transimpedance amplifiers, and analog-to-digital converters.

In this paper, we focus particularly on the DAC within the transmitter. In state-of-the-art coherent transmission systems, these converters are implemented using complementary metal–oxide–semiconductor (CMOS) technology and are monolithically integrated with the digital signal processor. The realization of DACs employs a parallelization approach, where the output signals from

parallel DACs are gradually serialized using analog multiplexers (AMUX), which are also implemented in CMOS. The achieved bandwidths and spectral efficiencies are relatively high, supporting the elevated data rates.

Currently, discussions are underway regarding the next generation of products, which aim to support transmission rates of 1.6 Tb/s [2]. These advanced systems will require a substantial increase in symbol rates from 130 to 240−260 GBaud. Consequently, the necessary electrical bandwidths will need to be increased to approximately 120−130 GHz. The realization of DACs with such bandwidths presents a significant challenge. Based on current architectures with parallel DACs and gradual serialization, this would involve both increased parallelization and extending serialization to much higher bandwidths at the output stage.

In addition to the monolithic integration of multiplexers in CMOS, there is intensive research into such components based on indium phosphide (InP) [3]–[9] and silicon-germanium [10]–[15] technologies. These multiplexers could be hybrid integrated with the DACs, thereby alleviating the demands on CMOS converters. The AMUXs must support both high bandwidths well beyond 100 GHz and high spectral efficiencies. Concepts such as time-domain multiplexing and frequency-domain multiplexing have been investigated, alongside parallelization as a critical parameter.

The hybrid integration of DACs and AMUXs requires a parallel data interface with two or four parallel data lines and a corresponding clock interface. In most publications, 2:1 multiplexing concepts are applied [7]–[15], where the required clock frequency for interfacing with CMOS application-specific integrated circuits (ASICs) would be extremely high. Alternatively, clock multipliers can be integrated into the AMUX [5] or greater parallelization can be chosen.

In this paper, we follow the idea of greater parallelization and investigate the extension of the 2:1 AMUX principle to a 4:1 AMUX. In Section II, a frequency-domain explanatory model based on the composition of the AMUX spectrum is introduced. Based on that model, the *N*-fold Nyquist frequency and the origin of unwanted signals are explained. Additionally, basic AMUX circuit concepts are discussed regarding their performance. For the most promising concept, a new extended 4:1 AMUX concept is proposed. Finally, Section IV shows new simulations and measurement results of a recent 2:1 AMUX realization.

II. FREQUENCY-DOMAIN EXPLANATORY MODEL OF THE AMUX

Figure 1a shows the operating principle of an *N*:1 AMUX, where a clock toggled switch periodically selects each of its *N* DAC input signals $x_n(t)$ during a sample time $T_{s,a}$, which is 1/*N* of each DAC's sample time $T_{s,d}$. Thereby the sample rate of the AMUX output signal $y(t)$ is *N* times higher than the DAC sample rate, i.e., $f_{s,a} = N f_{s,d}$. As shown in the following, by the *N*-fold sampling rate also the Nyquist frequency at the AMUX-output signal is *N* times the Nyquist frequency of the DAC input signals. Such DAC-AMUX setups are also called AMUX-DAC [16] or Super-DAC [17].

Figure 1a directly shows how the *N*-fold sample rate of the AMUX is achieved; however, it is not helpful to understand how the *N*-fold bandwidth is composed. Also, it neither shows how the signal spectrum of the AMUX is created nor how spectral noise impairs the AMUX's effective number of bits given by ENoB = (SINAD − 1.76)/6.02. To point out

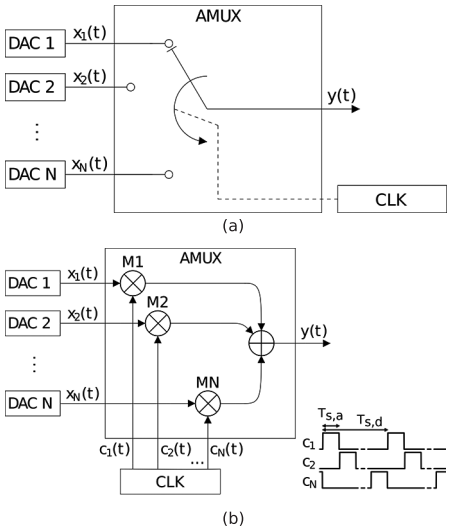

Fig. 1. (a) *N*:1 AMUX principle as a clocked toggle switch. (b) Illustration of the *N*:1 AMUX as mixers with added output [16]. In case of the 2:1 AMUX, only two, for the 4:1 AMUX, four mixers are present.

the origin of the main contributors to AMUX noise determined by the signal to noise and distortion ratio (SINAD), it is advisable to introduce a frequency-domain explanatory model of the AMUX, previously presented in [11] for a 2:1 AMUX, and to show how to expand this model to a 4:1 AMUX. As stated in [11], the effective resolution of the AMUX is mainly determined by three major impairments:

1. Since the AMUX-output spectrum is composed of the DAC spectra, the individual DAC's SINAD and therefore their ENoB strongly determines and limits the AMUX's ENoB.
2. Any non-linearity of the AMUX circuitry degrades the SINAD and ENoB by adding harmonics to the AMUX spectrum.
3. As shown by the frequency-domain explanatory model, the ENoB of the AMUX strongly depends on (a) a proper timing of the DAC signals and (b) identical DACs with identical signal paths up to the AMUX multiplexing core. In practical designs it turned out that there are multiple sources of impairments of (a) and (b) that are prone to severely degrade the AMUX's ENoB.

The frequency-domain explanatory model is based on the alternative AMUX block diagram in Figure 1b. There, the selection of the *n*th DAC signal, as shown in Figure 1a, is represented by the multiplication of the signal by a sampling signal $c_n(t)$ with a non-zero value during selection time. In the case of an ideal selection, $c_n(t)$ is periodic in $T_{s,d}$ and toggles between 1 (selection phase, i.e., sample time $T_{s,a}$) and 0 (not selected).

Ideally, the sampling signals are shifted and aligned in time, such that the individual DACs are evenly and sequentially selected. In case of a 2:1 AMUX, there are only two sampling signals $c_{1,2}(t)$, toggling between 1 and 0 with a 1:1 mark-space ratio and shifted by 180°. Due to the 1/0-toggling, $c_n(t)$ exhibits a non-zero DC component. Hence, the multiplication by $c_n(t)$ can be considered an unbalanced mixing of the DAC signals maintaining the baseband, consisting of the original DAC spectrum $S_{\mathrm{DAC}}(f)$, its replica $S_{\mathrm{DAC}}(f_{s,d}+f)$ at $f_{s,d}$, and its mirror-image $S_{\mathrm{DAC}}(f_{s,d}-f)$. Since the Nyquist frequency of the 2:1 AMUX is at $f_{s,d}$, only the original DAC spectrum and its mirror image contribute to the first Nyquist band of the AMUX output signal. These contributions are shown in the "baseband" and "mirror-image" columns in Figure 2. There, the baseband column displays the original DAC1,2 output spectra with their first two Nyquist bands up to $f_{s,d}$. Due to the unbalanced mixing of the AMUX, these spectra appear directly at the output and are marked by M1,2 according to the mixer

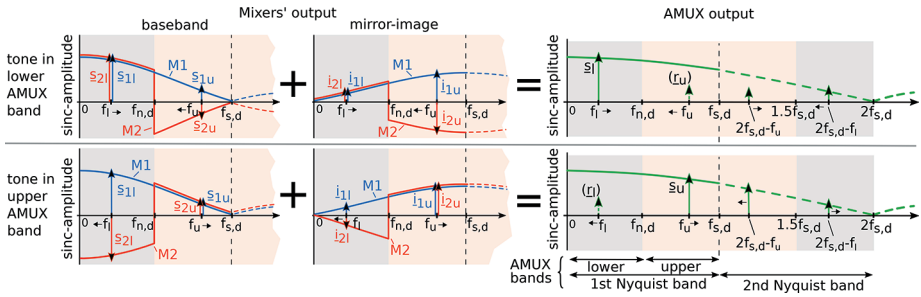

Fig. 2. Spectra at the AMUX-output of a 2:1 AMUX.

of the respective input. Considering zero order hold (ZOH) DAC signals, the DAC output amplitude drops by $\mathrm{sinc}(f/f_{s,d})$: = $\sin(\pi f/f_{s,d})/(\pi f/f_{s,d})$ to sinc ½ ≈ 63.7 % (−4 dB) at the DAC Nyquist frequency $f_{n,d} = f_{s,d}/2$, and to zero at $f_{s,d}$. This behavior is shown by the sinc-envelope of the M1,2 signal amplitude in Figure 2. The second DAC signal is shifted against the first one by $T_{s,a} = T_{s,d}/2$ (i.e. 180°) to align the center of their ZOH signal to the sampling pulses $c_{1,2}(t)$. The 180° phase shift of the second DAC signal leads to a sign change in its second Nyquist band in the M2 spectrum, shown by inversion of the sinc-envelope in Figure 2. The mirror image of the baseband at $f_{s,d}$ is shown in the second column of Figure 2 by its mirrored sinc-envelope. Because of the respective phase shifts of the sampling signals, for those mirror images the same sign considerations hold as in the baseband. Higher order images also contribute to the output signal, but due to their sinc weighting, they are of minor influence.

To show how a tone of a certain frequency is created, the AMUX output spectrum can be subdivided into a lower and an upper AMUX band, as defined in Figure 2, that correspond to the first two Nyquist bands of the DAC signals. Hence, a tone at f_l, f_u generated in the lower/upper AMUX band comes with an alias tone at $f_{s,d} - f_l, f_{s,d} - f_u$ in the upper/lower AMUX band, respectively. In Figure 2, the baseband tones are depicted by phasors $\underline{s}_{1,2l}$ and $\underline{s}_{1,2u}$ for the lower and upper band of M1,2. Phasors pointing up/downwards exhibit a 0°/180° phase shift, respectively. The respective image phasors are represented by phasors $\underline{i}_{1,2l}$ and $\underline{i}_{1,2u}$. The two rows of Figure 2 illustrate tone generation for both lower and upper AMUX bands. For a generation of a tone at f_l in the lower band, the two DACs have to output signals in phase (i.e. in the first Nyquist band of the DACs), while they are of opposite phase for a tone at f_u in the upper band.

The final AMUX output signal constitutes of the superposition of the baseband and mirror image signals in either row of Figure 2. Ideally, the intended tones superimpose constructively, while the alias tones cancel out. The superposition of the baseband and mirrored $\mathrm{sinc}(f/f_{s,d})$ envelopes results in a total $\mathrm{sinc}(f/(2f_{s,d}))$ envelope as shown in the right column of Figure 2. Because of this sinc-envelope and an AMUX output 1st Nyquist bandwidth of twice the DACs' 1st Nyquist bandwidth, the 2:1 AMUX output mimics a Super-DAC with doubled sampling rate.

In the presence of amplitude or timing mismatches of the respective data and sampling signals, residual tones $\underline{r}_{l,u}$ persist in the output signal. Those residual tones originate from imperfect cancellation in amplitude or phase of the alias tones and can be caused by multiple sources in the AMUX setup. For high signal path

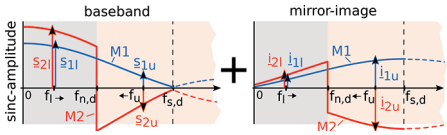

Fig. 3. Example of an amplitude mismatch.

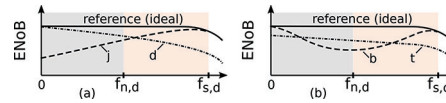

Fig. 4. Basic types of ENoB vs. frequency characteristics of a 2:1 AMUX. (a) Diverged, d-type, and joined, j-type. (b) Tilted and translated, t-, and bathtub, b-type [11].

linearity and high SINAD DAC signals, they become the dominant impairment on AMUX resolution. As an example shown in Figure 3, an amplitude mismatch between M1,2 inputs is considered for lower band tone generation. This mismatch can originate from different DAC amplitudes or a gain mismatch along the AMUX signal paths. In the shown case, M2 exhibits a higher amplitude. For the wanted tone, the higher M2 amplitude increases the baseband $|\underline{s}_{2l}|$ as well as the mirror image amplitude $|\underline{i}_{2l}|$ and thus the total output amplitude, which still approximately follows a sinc-envelope. For the alias tone, the M1,2 tones retain their respective 0°/180° phase but exhibit different amplitudes; thus, their sum is nonzero, whereby a residual tone remains. The SINAD used for ENoB calculations depends on the ratio of the wanted signal and the residual tone. Depending on the amplitude progression of wanted and residual tone along the baseband and mirror-image sinc-envelopes, characteristic ENoB vs. frequency traces are created. In the example of the amplitude mismatch in Figure 3 the ratio between wanted and residual tone amplitude increasingly decreases over frequency. This holds especially for tones in the upper AMUX band, where the sinc-envelope for the residual tones reaches its maximum for $f_u = f_{s,d}$. This behavior results in t-type ENoB characteristic [11] shown in Figure 4. To minimize the amplitude mismatch, a symmetrical AMUX circuit design as well as matched DAC signal paths are important. Analogous to the amplitudes, also the signal and clock phases have to exactly match the 0°/180° relation to cancel out perfectly. As shown in [11], any imperfection causes one of the ENoB characteristics in Figure 4, where (d) and (j) are related to clock offset and delay, respectively, whereas (b) relates to imperfections in the clock-to-signal timing, and signal-to-signal timing. The individual characteristics of wanted and residual tones of these characteristics are utilized in [11] to develop tailored calibration routines for the AMUX setup.

To extend the frequency-domain model in Figure 2 to a 4:1 AMUX, the model needs to be adapted to the differences between 2:1 and 4:1 versions of the AMUX. However, for the DAC signals, generally, the same ZOH sinc-envelope properties as for the 2:1 AMUX are considered. In favor of clarity, in the baseband column of the 4:1 AMUX spectra in Figure 5, only two out of four DAC input signals are shown in one diagram. Thereby, the total of four signals are shown in the two diagrams on top of one another. Also, only one example is given for the tone generation in the lowest (first out of four) AMUX band. For the 4:1 AMUX, the baseband spectrum $S_{\mathrm{DAC}}(f)$, as well as the mirror-image $S_{\mathrm{DAC}}(f_{s,d} - f)$, its replica $S_{\mathrm{DAC}}(f_{s,d} + f)$, and the second mirror image $S_{\mathrm{DAC}}(2f_{s,d} - f)$ contribute to the first AMUX Nyquist band. As the sample time $T_{s,a} = T_{s,d}/4$ is halved compared to the 2:1 AMUX, also the related phase shifts in the four AMUX bands are halved. While the time shifts and properties of M1,3 are the same as for M1,2

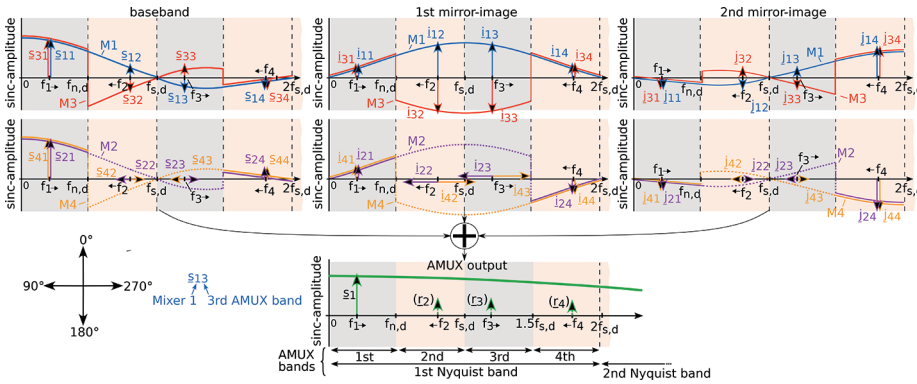

Fig. 5. Composition of the AMUX-output spectrum of a 4:1 AMUX for a tone f_1 in the first AMUX band. The frequencies f_2, f_3, and f_4 are the alias tones in the other AMUX bands. The $\underline{i}$ and $\underline{j}$ represent first and second mirror-image tones, respectively. Dotted lines for M2,4 represent the sinc-envelopes phase-shifted by 90°/270° in the up/downward direction.

of the 2:1 AMUX, for every second input signal (M2,4 in Figure 5), 90° and 270° phase shifts occur in the second and third AMUX bands. Due to the shortened sampling pulses compared to the 2:1 AMUX, the output amplitude follows a $\mathrm{sinc}(f/(4f_{s,d}))$ envelope. In the example in Figure 5, it can be seen that at the wanted tone in the first AMUX band, all four baseband signals superpose constructively, while in the other AMUX bands, the signals cancel out each other. For this example, in the second and third bands, M1,3 cancel out due to respective 0°/180° phase shifts. Also, M2,4 exhibit 90°/270° phase shifts and cancel out, respectively. In the fourth AMUX band, M1,3 have the same phase of 0° and superpose constructively, while M2,4 exhibit 180°, canceling out corresponding M1,3 alias tones. For an imperfect alias tone cancellation, a total of three residual tones can occur for the 4:1 AMUX.

As there are double the inputs and up to three instead of one residual tones compared to the 2:1 AMUX, the calibration of a 4:1 AMUX measurement or simulation is even more complex. Like for the 2:1 AMUX, the origins of wanted and unwanted tones and their sinc-related frequency dependency of their amplitudes are valuable insights for ENoB optimization in the current 4:1 AMUX development.

III. 2:1 AND 4:1 AMUX CIRCUIT CONCEPTS

Multiple concepts to realize the AMUX function are present in literature. These are either based on frequency-domain or time-domain multiplexing [16]. Since the latter is comparatively easy to realize and does not need for any challenging amplitude and phase alignments across the interleaved frequency bands, we focus here on the time-domain approach.

Most time-domain 2:1 AMUX concepts combine two DAC inputs to one output signal, acting like the toggle switch in Figure 1a. The two main toggle switch concepts are based on Gilbert cells and are named clocked-TAS and clocked-SEL, respectively [11]. In the clocked-SEL concept, shown in Figure 6 for the 2:1 AMUX, two linear transadmittance stages (TAS) are biased via constant currents I_0 and driven by DAC signals. The TAS output currents are switched

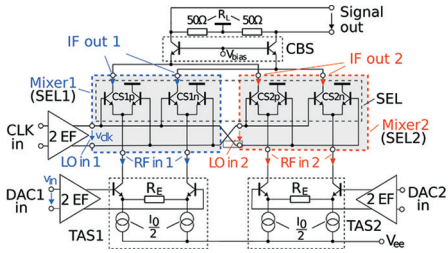

Fig. 6. Circuit principle of the 2:1 AMUX core realized by the clocked-SEL concept.

by selector stages (SEL), which consist of two current switches (CS), each. Those SEL switch the data signals either to the output or to the ground. All inputs incorporate emitter followers, while the output is buffered with a common base stage (CBS). In contrast, the competing clocked-TAS concept (cf. [4]–[6]) switches the TAS bias currents, so that only one of the two TASs is turned on at a time and contributes to the output signal. In [11], it is shown that the effective resolution achievable with this concept is strongly suffering from dynamic currents through the non-linear base-emitter junction capacitance of the TAS transistor. Therefore, in the following, the clocked-SEL is preferred over the clocked-TAS.

The multiplication of the input signal by a sampling signal $c_n(t)$ as introduced in Figure 1b is realized by driving the SEL by a clock voltage v_{clk} at a frequency of $f_{clk} = f_{s,d}$. The sampling signals $c_n(t)$ do not directly represent physical voltages or currents; they rather describe the 1/0-toggling function carried out by the CS/SEL stages. Due to the steep transfer function of a CS, it basically switches its input current at the common emitter node to either of its two outputs depending on the sign of v_{clk}. In case of the 2:1 AMUX, this leads to the data signals being switched alternately and symmetrically with a duty cycle of 1/2 to the output or ground. By inversion of the two clock signals at the respective SEL, only one of the two data signals is present at a time at the AMUX output.

For a higher order AMUX ($N > 2$), also only one data signal at a time is supposed to be present at the output. Thus, the sampling pulses have to be shortened to the AMUX sample time $T_{s,a} = T_{s,d}/N$. This corresponds to a duty cycle of $1/N$ for the sampling signals. Figure 7 proposes a 4:1 AMUX circuit using the clocked-SEL concept. It basically consists of two of the 2:1 AMUX cells of Figure 6, whose output currents are summed up by only one CBS. The SEL2,4 are driven by clock signals shifted by 90°/270° compared to SEL1,3, which need 0°/180° as for the 2:1 AMUX. The lower duty cycle is achieved by the introduction of an offset (OS) to the clock voltage at each SEL (cf. "OS"-input at the driving EF stages). This shortens the time where $v_{clk} > 0$ and thereby reduces the sampling time of the SEL. Assuming sinusoidal clock signals, an offset V_{os} related to the clock amplitude

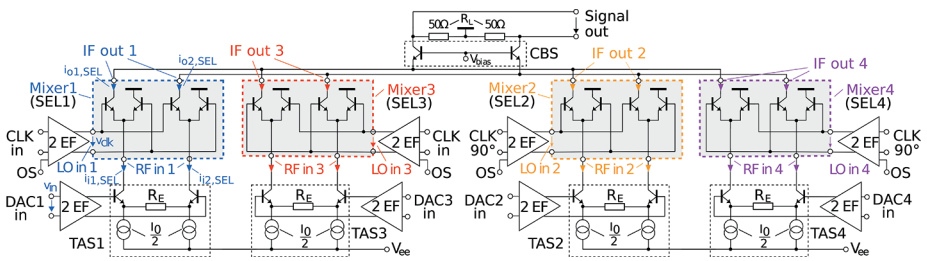

Fig. 7. Circuit principle of the proposed 4:1 AMUX core realized by the clocked-SEL concept.

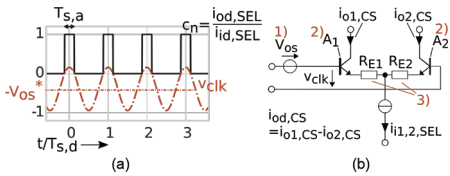

Fig. 8. (a) Clock voltage with offset and resulting idealized sampling signal $c_n(t)$ for a 4:1 AMUX. (b) Three methods to introduce an offset to the transfer characteristic of a CS by (1) offset voltage V_{os}, (2) different transistor areas A_1, A_2, or (3) different emitter degeneration resistors R_{E1}, R_{E2}.

V_{clk} by a factor of $V_{os}/V_{clk} = \cos(\pi/N)$ is needed to achieve a duty cycle of $1/N$. For the case of the 4:1 AMUX shown in Figure 8a, this ratio yields $\sqrt{2}/2 \approx 70.7\%$. It is important to note that this offset depends on the amplitude and the signal shape of the clock signal and is thereby a crucial parameter in design optimization.

In Figure 8b, three different methods to generate the needed offset for a CS are suggested: (1) direct application of an offset voltage V_{os}, (2) transistors with different emitter areas A_1, A_2, and (3) different emitter resistances R_{E1} and R_{E2}. The proposed methods combined contribute to an effective offset voltage of the SEL-CSs

$$V_{OS}^{*} = V_{OS} + V_T \ln\frac{A_2}{A_1} + \frac{R_{E1} - R_{E2}}{2} i_{i1,2,SEL}, \quad (1)$$

where $i_{i1,SEL}$ and $i_{i2,SEL}$ are the TAS output currents at the emitter node input of the respective SEL-CS. If eqn (1) is considered in the transfer characteristic of a SEL-CS, the offset becomes dependent on those actual current values, which result in a non-linear offset and transfer characteristic. In case of only methods (1) and (2) (i.e. $R_{E1} = R_{E2} = 0$) in eqn (1), the single-ended current transfer function

$$\frac{i_{o1,2,SEL}}{i_{i1,2,SEL}} = \frac{1}{2}\left(1 + \tanh\left(\frac{V_{clk}\cos(2\pi f_{clk}t) - V_{OS}^{*}}{2V_T}\right)\right) \quad (2)$$

does not depend on the actual current value, so that the SEL-CS sampling linearly transfers the sample values. Due to the sampling linearity, the single-ended expression in eqn (2) can analogously be expressed for the differential output current of the SEL. However, the size factor A_2/A_1 becomes impractical as due to the logarithm, very large factors (e.g. > 10^5 for V_{clk} = 500 mV) are needed to get usable offsets. Hence, the only reasonable approach to generate the needed offset is to apply offset voltages directly to the clock inputs.

IV. SIMULATION AND MEASUREMENT OF A 2:1 AMUX

The following measurement results are obtained from a 2000 × 900 µm sized AMUX chip realized in IHP SG13G2 technology with f_T = 300 GHz and f_{max} = 500 GHz [21]. The simulated current consumption is 648 mA/35 mA at its two supply voltages of −5.5 V/−2.5 V, respectively. Due to on-chip supply voltage issues, the total measured power consumption is raised by about 30% up to 4.7 W. Nevertheless, the chip shows results good enough to be published, because its ENoB is only marginally lower than the highest reported ENoB in [10] but at a higher sampling rate and with significantly higher clock- and data-path bandwidths (cf. Table I). Furthermore, the AMUX, completely packaged in an RF-module, achieves the highest reported maximum sample rate of 186 GS/s for an SiGe module. Figure 9a shows the layout of the AMUX chip that follows the cell-based design approach introduced in [22]. The high number of pads is used to adjust the currents of the transistor stages and determines the chip size. The clock amplifier chain incorporates three clock buffers and conditions the clock signal for the 2:1 AMUX cell. The AMUX cell

TABLE 1
STATE OF THE ART

	Technology (f_T,f_{max})/GHz	Sampling rate	ENoB at (f_{low} –f_{high})***	Bandwidth clock path	Bandwidth signal path	Diff. output voltage swing	Power/supply voltage
[4]	0.5 µm-InP(290/320)	80 GS/s	–	50 GHz	–	–	0.5 W/ –4.5 V
[5]	0.5 µm-InP(290/320)	128 GS/s	–	64 GHz	67 GHz	0.5 V_{pp}	0.54 W/ –4.5 V
[6]	0.25 µm-InP(460/480)	168 GS/s**	–	99 GHz	> 110 GHz	1.5 V_{pp}	0.9 W/ –4.5 V
[18]	0.7 µm-InP(340/410)	100 GS/s	–	–	–	1.1 V_{pp}	–
[19]	0.13 µm-SiGe(300/500)	56 GS/s*	–	60 GHz*	> 67 GHz*	0.75 V_{pp}	1.06 W/ –4.5 V
[14]	0.13 µm-SiGe(470/650)	190 GS/s* **	–	–	> 110 GHz*	1 V_{pp}	1.5 W/–
[20]	55 nm-SiGe(320/370)	100 GS/s	4.9–4.25	≥ 50 GHz	73 GHz	0.4 V_{pp}	0.7 W/ 2.5 V
[10]	55 nm-SiGe(325/375)	120 GS/s	7.7–4.1	64 GHz	50 GHz	0.7 V_{pp}	2.17 W/ –5.7 V
This work	0.13 µm-SiGe(300/500)	186 GS/s****	7.1–3.7	> 70 GHz	> 70 GHz	1.2 V_{pp}	4.7 W/ –5.5 V

* Measured on chip. ** Using pre-filtered input signals. *** f_{low} /f_{high} is the smallest/highest measured frequency for the ENoB. (**** For PAM-2).

Fig. 9. Chip layout (a), AMUX IC bondwire assembly (b), and RF-module (c).

itself is designed using the clocked-SEL principle as high linearity was the primary concern of the design. Data signals are buffered by input amplifiers, while the AMUX cell is placed in close vicinity to an output amplifier and the chip output, to keep the high-speed signal path short. Figure 9b,c show the chip bondwire and RF module assembly following the principle described in [23]. Target specification for the 2:1 was a maximum sampling rate exceeding 120 GS/s, while maintaining an ENoB of 6 bit. Figure 10a shows on the left the simulated ENoB and amplitude curves for the AMUX at 128 GS/s. On the right hand side, the measured ENoB and amplitude curves are shown. Measurements were carried out using two 8-bit MICRAM DAC5 AWG modules for signal generation, a Keysight E8257D analog signal generator for clock signal generation that drives both AMUX and DAC clocks, and a Keysight N1000A DCA-X sampling oscilloscope, respectively. No digital corrections or data pre-emphasis were applied to any of the measurements. The

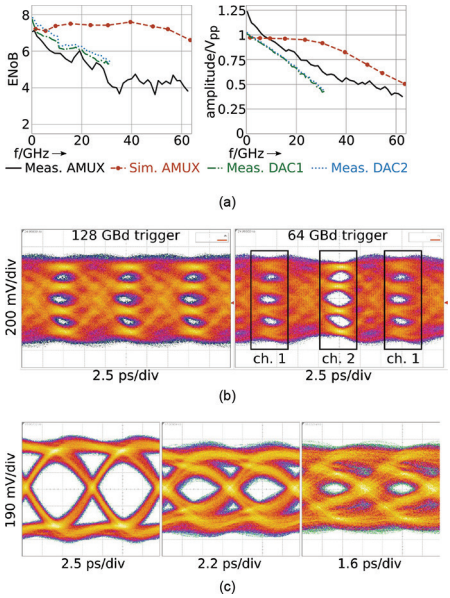

Fig. 10. (a) ENoB and amplitude curves at 128 GS/s. (b) PAM-4 128 GS/s eye diagrams, triggered to 128 GBaud (left) and triggered to 64 GBaud (right). (c) PAM-2 eye diagrams for 120/140/186 GS/s, respectively.

AMUX reaches an ENoB of 7.1 bit for the lowest output frequency, dropping to a minimum of 3.7 bit at 49 GHz. The ENoB curve basically follows the DAC ENoB curve in the lower AMUX band, which is also shown for reference in Figure 10a. It drops relatively fast from 7.1 bit to about 4 bit at a middle output frequency. For higher frequencies, it remains quite constant between 3.7 and 5 bit. Figure 10b shows measured PAM-4 eye diagrams for the AMUX at 128 GS/s. On the left side of Figure 10b, eye diagrams triggered at 128 GS/s are shown. The eye diagrams shown on the right side were triggered at 64 GS/s, showing the two corresponding data channels, alternately. Both channels exhibit different eye openings, which is likely due to a thermal asymmetry in the AMUX chip caused by the increased current consumption. However, the eye opening of channel 2 promises an upward potential if the supply voltage issue was fixed. Finally, Figure 10c shows PAM-2 eye diagrams up to the operating limit of 186 GS/s.

V. CONCLUSION

In this paper, we presented considerations to extend the 2:1 AMUX concept to a 4:1 AMUX. The frequency-domain explanatory model introduced in [11] was extended to the 4:1 AMUX, giving valuable insights for the ENoB calibration of simulation and measurements. Also, for the 4:1 AMUX, a new circuit concept based on the clocked-SEL was shown, providing a new approach for future AMUX designs. Finally, we showed measurements of a 2:1 AMUX module exhibiting a leading maximum ENoB of up to 7.1 bit at 128 GS/s and a maximum sample rate of 186 GS/s.

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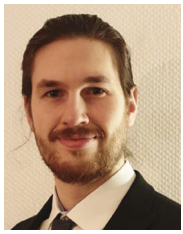

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