B55X: A SHIFT in STMicroelectronics BiCMOS Technologies

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Abstract—**The SHIFT (Sustainable tecHnologies enablIng Future Telecom applications) project funded by Chips JU and National Authorities partly supports the qualification towards the production of STMicroelectronics BiCMOS055X, which is one of the key technologies evaluated in this project. This paper examines why BiCMOS055X is also a significant shift in STMicroelectronics BiCMOS offer, first in terms of innovation and performances, but also with respect to the device offer that has been tailored to address different applications, turning out in a versatile technology offer.**

Index Terms—**BiCMOS, silicon germanium, HBT, RF, THz, communication, optical, wireless, Satcom.**

I. INTRODUCTION

The first consumer market of silicon germanium (SiGe) BiCMOS technology was the radiofrequency (RF) transceiver of cellular phones about 20 years ago. This application, as the TV tuner one, has been progressively captured by complementary metal–oxide–semiconductor (CMOS) technology [1], which is currently happening for automotive radars. On the other hand, whereas the RF performance of CMOS does not improve anymore, applications served today by SiGe BiCMOS, i.e., RF front-end modules (FEM) and optical transceivers, benefit from the intrinsic superiority of the SiGe heterojunction bipolar transistor (HBT) [2]. In addition, there are perspectives to improve performances of SiGe HBT beyond what is currently being qualified for production [3][4]. However, although the RF performance of the overall platform, i.e., including all the devices, is of paramount importance, technological complexity and related cost must not be neglected. It is increasingly challenging to serve multiple applications featuring different cost/performance trade-offs. Indeed, low earth orbit (LEO) satellite communications (Satcom) in Ku and Ka bands, i.e., between 10 and 40 GHz, which generate consumer-like production volumes [5], put severe constraints on wafer cost, while being quite demanding on performance. Optical transceivers, whose demand is expected to increase with the emergence of artificial intelligence (AI) clusters [6], and targeted data rates for next generations are 200 and 400 G per lane, require additional options. Finally,

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RF FEMs for future 5G+ and 6G wireless communication infrastructures push the technology to its operation frequency limits, which is today the D-band, i.e., between 140 and 170 GHz. Practically, the core of the technology, and more especially the SiGe HBT architecture, is not modified to address the different applications although the transistor is used at very different bias conditions. But the technology content must be adapted to get the best well-known power–performance–area–cost (PPAC) key performance indicator (KPI). The "S" of "sustainability," a priority for STMicroelectronics (ST) [7], must be added. It is also part of the SHIFT (Sustainable tecHnologies enablIng Future Telecom applications) project [8], which relies on BiCMOS055X (B55X) technology. B55X, which serves the Move2THz [9] project too, is the topic of this paper. The first part reviews the history of silicon germanium BiCMOS technology development at ST. It allows understanding, in the second part, why B55X is a disruptive technology in the ST roadmap with respect to innovation, performance, and versatility. The third part discusses the positioning of this technology versus the current state-of-the-art. Finally, the key points of the technology are summarized in the conclusion and perspectives for next generations are drawn.

II. HIGH-SPEED SIGE BICMOS TECHNOLOGIES HISTORY AT STMICROELECTRONICS

ST holds 25+ years of experience in SiGe BiCMOS illustrated in Figure 1, showing the increase of SiGe HBT speed over the generations and how it has been combined with the CMOS nodes to serve different markets. It started with a 0.35-µm BiCMOS technology (BiCMOS6G) [10] and continued with two generations in 0.25 µm (BiCMOS7 [11] and BiCMOS7RF [12]) and two generations in 0.13 µm (BiCMOS9 [13] and BiCMOS9MW [14]). These technologies were developed on 200-mm wafers. The sixth and seventh generations are based on 55-nm CMOS and thus migrated to 300-mm wafers, first with BiCMOS055 [15] and now with BiCMOS055X [16]. Table 1 summarizes the main process differences between the generations.

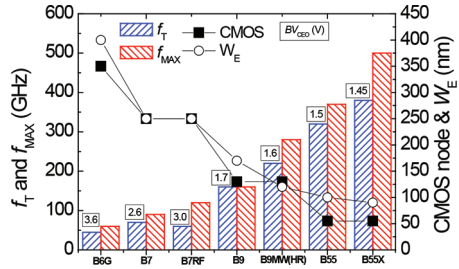

Fig. 1. STMicroelectronics high-speed SiGe BiCMOS technologies (HBT performance & CMOS node). W_E is the physical emitter width. BV_{CEO} is the emitter–collector breakdown voltage of the HBT with an open base. f_T and f_{MAX} correspond to the peak values measured for the SiGe HBT.

Beyond the CMOS node, which did not always change between two generations, the SiGe HBT architecture evolved continuously. It started from a quasi-self-aligned (QSA) single-polysilicon (SP) architecture using a non-selective epitaxy growth (NSEG) of the SiGe base [10]. This architecture was simple but suffered from several limitations, the main one being related to the implantation of the extrinsic base. The second generation of SiGe HBT solved this issue with the introduction of a double-polysilicon (DP) architecture [11]. In addition, the introduction of carbon in the base [12] and deep trenches isolation (DTI) helped to further improve the performance. The full self-alignment (FSA) between the emitter and the base, a major step in base resistance (R_B) reduction [17], was brought by the third generation [14][15].

TABLE I
DIFFERENCES BETWEEN STMICROELECTRONICS BICMOS TECHNOLOGIES

Technology		B6G	B7	B7RF	B9	B9MW		B55	B55X
CMOS node (nm)		350	250	250	130	130		55	55
Bulk substrate resistivty		SR	SR	SR	SR	SR	HR	SR	SR
SiGe HBT architecture	**Emitter-Base**	QSA-SP		QSA-DP		FSA-DP			EXBIC
	Intrinsic base epitaxy	NSEG SiGe		NSEG SiGe:C		SEG SiGe:C			
	Extrinsic base epitaxy	No							Yes
	Collector epitaxy	NSEG							SEG
	DTI	No		Yes					Optional
BEOL		Digital (native)		Thick Cu	Digital (native)	Optimized for RF (Thick Cu native)			

It was achieved by moving to the selective epitaxial growth (SEG) of the base. The fourth generation addressed the critical point of the intrinsic-to-extrinsic base link resistance using a specific epitaxy process step. It is achieved with the EXBIC (*Epitaxial eXtrinsic Base Isolated from the Collector*) architecture developed for the B55X technology [18]. As illustrated in Figure 1, where emitter–collector breakdown voltage (BV_{CEO}) evolution is shown, peak frequency increases have been achieved at the expense of the breakdown voltage (collector doping is increased to delay the onset of the Kirk effect). However, it decreased much less than peak frequencies increased. In addition, the base–collector breakdown voltage (BV_{CBO}), the maximum voltage at which the transistor can be biased, is about 3–4 times higher than BV_{CEO}.

Last, but not least, a major evolution appeared in the backend of line (BEOL), i.e., the metallization stack, with the introduction of thick copper module(s). It became standard starting from the B9MW technology [14], but an ultra-thick Cu option has been developed in B7RF [12]. The combination of ultra-thick via(s) and line(s) allows decreasing metal resistances and move away RF passives from the substrate, reducing substrate losses and so improving RF passive performances. The use of a high resistivity (HR) substrate does not always solve the limitation of standard resistivity (SR) substrate, as parasitic conduction layer can appear during the process. However, the HR substrate is appealing to integrate high-performance switches [19]. Benefits of RF optimized BEOL are extensively discussed in Section III.B

III. BICMOS055X: A DISRUPTIVE TECHNOLOGY IN ST ROADMAP

As shown in Table 1, the B55X technology gathers several innovations compared to the previous nodes. In addition, the technology has been defined to provide a versatile offer to serve multiple applications.

A. An innovative SiGe HBT architecture

Although the double-polysilicon self-aligned (DPSA) architecture using

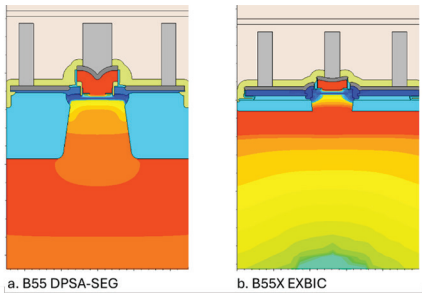

Fig. 2. TCAD cross-sections of the DPSA-SEG (a) and EXBIC (b) architectures used in STMicroelectronics B55 [15] and B55X [16][18] technologies, respectively.

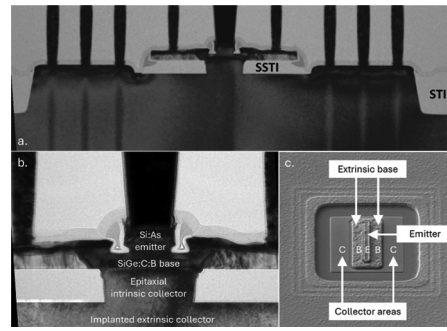

Fig. 3. B55X SiGe HBT (EXBIC architecture: TEM cross-sections at the end of fabrication of the whole transistor (a) and zoom-in of the emitter–base area (b) [18] and SEM top view after extrinsic base patterning (c).

an SEG of the base brought a significant improvement of R_B (thanks to the emitter–base self-alignment), further reducing this resistance collides with the way the link between the intrinsic base and the extrinsic base is made. Indeed, this link is done during the SEG of the base, leaving little room to optimize independently the intrinsic and extrinsic parts of R_B [20]. This issue is addressed with the last generations of architecture featuring a dedicated epitaxial growth of the extrinsic base [3]. Such a step is implemented in B55X [18] and combined with an innovative collector module featuring super shallow trench isolation (SSTI) and a shallow extrinsic collector layer, visible in Figures 2 and 3. It allows getting rid of DTI that are no longer required, neither to increase device compactness nor to reduce the collector–substrate (C_{CS}) capacitance [16]. An important point compared to similar collector architectures [3] is the use of standard transistor layout for which the emitter length of several micrometers can be drawn and the use of unit cells is not mandatory to increase the device area. This is illustrated by the CBEBC layout (i.e. 2 collector contacts "C" and 2 base contacts "B" on each side of the emitter contact "E") shown in Figure 3c. In addition, the height of the EXBIC architecture has been reduced compared to the DPSA-SEG architecture (cf. Figure 2), which is favorable for the emitter resistance R_E and opens its integration in a more advanced CMOS node [21]. f_T and f_{MAX} peak frequencies reported in Figure 1 are important KPIs, providing information on the maximum operation frequency and the gain that can be achieved at a given frequency. Another important KPI for low noise amplifier is the minimum noise figure (NF_{MIN}) that is known to correlate with f_{MAX} since it depends partly on same

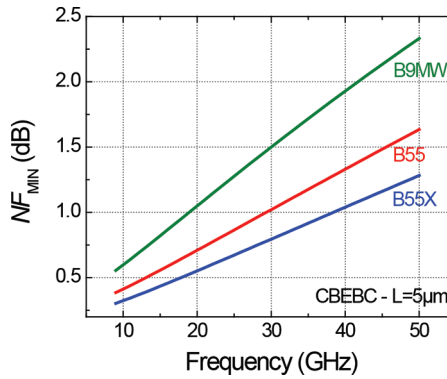

Fig. 4. Comparison of the evolution of SiGe HBT noise figure with the frequency (CBEBC transistor, V_{BE} = 0.82 V) between B9MW, B55, and B55X (data are from the models).

TABLE 2
B55X CMOS DEVICES OFFER

Gate oxide	Devices	Minimum L_G (nm)	nMOS	pMOS	RF model
5 nm	GO2 CMOS	280	SVT	SVT	Yes
1.8 nm	LP CMOS	60	LVT	LVT	Yes
			SVT	SVT	Yes
			HVT	HVT	No
	HPA CMOS	140	HPA	HPA	Yes
	LP SRAM	70	SVT	SVT	NA
			HBT	HBT	NA
1.3 nm	GP CMOS	45	LVT	LVT	Yes
			SVT	SVT	Yes
			HVT	HVT	No

parameters, a key one being R_B. Figure 4 compares the evolution of NF_{MIN} with the frequency between B55X and the two previous generations (B55 and B9MW). B55X SiGe HBT exhibits a strong reduction of the noise figure compared to previous generation with NF_{MIN} values below 0.5 and 1.0 dB in Ku and Ka bands, respectively. These values represent the current state-of-the-art [18].

B. Versatile CMOS and BEOL offers

Innovation in B55X does not only lie in SiGe HBT architecture but also in the definition of the technology content and its versatility to meet the PPACS (cf. Section I) of each application. The main changes compared to the previous generation are the ability to select a reduced list of CMOS devices and several BEOL stacks.

Table 2 presents the list of metal–oxide–semiconductor (MOS) devices available both in B55 and B55X. While the three families of MOS transistors (corresponding to the three-gate oxide thicknesses) could not be separated in B55 (only some device V_T flavors are optional), they can be selected separately in B55X. Four-gate oxide options are possible in B55X:

- 5-nm CMOS only;
- 1.8-nm CMOS only;
- 5-nm CMOS + 1.8-nm CMOS;
- 5-nm CMOS + 1.8-nm CMOS + 1.3-nm CMOS.

Process flow, and more especially the gate oxidations scheme, has been defined to insure a full compatibility between the options. RF model is available for most of the CMOS transistors.

Figure 5 presents the different metallization stacks developed for the B9MW, B55, and B55X technologies. They exhibit one or even two ultra-thick Cu layers of 2.3 or 3 µm combined with ultra-thick vias of 1.5 or 2.7 µm and feature different numbers of thin and thick metal layers. It allows addressing different trade-offs between the RF performance of inductors and transmission lines (related to the thick metal layers), the digital performance (related to the thin metal layers) and the process cost, i.e., overall the technology competitiveness. The Q-factors of single and differential ended inductors of 300 and 800 pH at 10, 20, and 40 GHz are reported in Figure 6. As expected, the thicker is the stack, the better is the quality factor and selecting the right stack is a

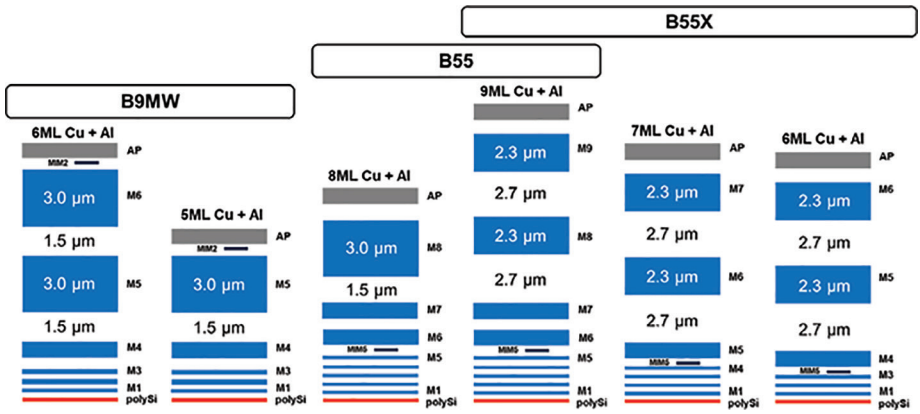

Fig. 5. Metallization stacks developed in the B9MW, B55, and B55X technologies.

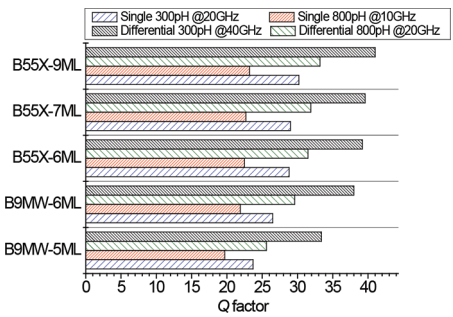

Fig. 6. Comparison of performance (Q-factor) of single ended and differential inductors of the BEOL stacks of Figure 5.

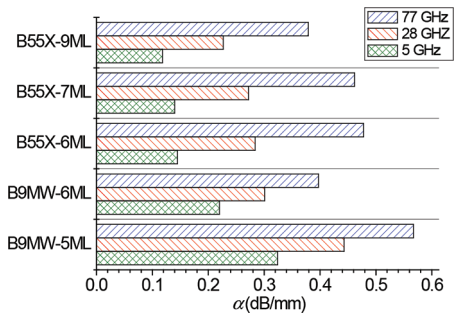

Fig. 7. Comparison of performance (attenuation constant α) of transmission lines of the BEOL stacks of Figure 5 (Z_c = 50W).

trade-off between wafer cost and circuit performance. However, it is interesting to note that the penalty of using a 5 Cu ML instead of 6 in B9MW is low at 10 GHz, while this difference is larger at 40 GHz. Also, performance is always better with B55X dual thick Cu stack, with a very low impact of the number of thin metal layers. Figure 7, showing the attenuation constant (α) of transmission lines at 5, 28, and 77 GHz for the same BEOL stacks, exhibits the same conclusions with respect to the importance of dual thick Cu module at higher frequencies and the low weight of the thin metal layers. Finally, although thin metal layers are thinner in B55X than in B9MW (in line with the digital density difference of the CMOS node), performances of inductors and transmission lines are always better (whatever the frequency) in B55X 6ML than in B9MW 6 ML. This is thanks to the thickening of the ultra-thick via + metal module in B55X (5 µm vs. 4.5 µm in B9MW), which represents a major breakthrough in the via thickness compared to previous generations.

III. BICMOS055X VERSUS THE COMPETITION

It is clear from previous sections that B55X features the best performance of the BiCMOS technologies developed at

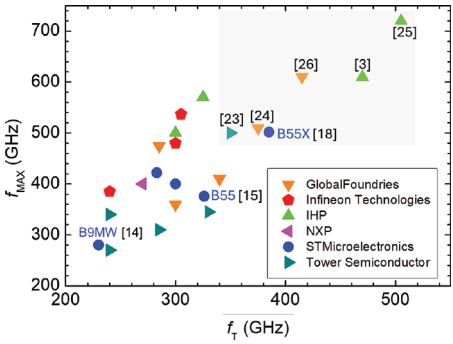

Fig. 8. Peak f_T and f_{MAX} values of high-speed SiGe HBT technologies (references are provided for f_T > 350 GHz and f_{MAX} > 400 GHz and ST technologies).

ST while taking care to adapt the technology offer to the needs by offering many options. However, its competitiveness can only be evaluated according to the competition. While there are only a few data published on metal stacks [22] and relative passive devices performance, SiGe HBT results are commonly reported. Figure 8 compares SiGe HBT f_T and f_{MAX} from different players with top performances (f_T > 350 GHz and f_{MAX} > 450 GHz) highlighted with a gray background. State-of-the-art technologies in production for about 10 years exhibit f_T and f_{MAX} of ~300 and ~400 GHz, respectively (± 50 GHz). B55X belongs to a new generation of technologies using an epitaxial base link aiming at dramatically reducing R_B, leading to f_{MAX} > 450 GHz that could not be achieved in previous generations. Looking at the area highlighted in gray, B55X [18] appears in the low f_T/f_{MAX} corner, very close to [23] and [24]. Best performance [25] has been demonstrated in a bipolar-only process, i.e., not compatible with CMOS, the CMOS compatibility being recovered in [3] for a 130-nm node (with an aluminum BEOL). CMOS node (and related substrate) is indeed an important difference between these "top" technologies. While [23] is based on 180-nm CMOS, [24] and [26] results are obtained on a 45-nm CMOS, built on partially depleted silicon-on-insulator substrate, which represents the current CMOS state-of-the-art in BiCMOS. Of course, it comes with a higher complexity/cost compared to 55-nm bulk CMOS.

IV. CONCLUSION

In the recent past years, SiGe BiCMOS development has been driven by the increase of the SiGe HBT RF performance on the one side and the move to more advanced CMOS nodes on the other side. The CMOS roadmap of these technologies was driven by some demanding applications, optical communications being the main one. While nanoscale nodes exhibit clear advantages [21], there is no high-volume application today calling for the integration of SiGe HBT with very advanced CMOS. On the contrary, the LEO Satcom application that drives the production volumes today requires a moderate CMOS density. In this context, a 55-nm node appears as a sweet spot regarding the CMOS performance and complexity. The combination of this CMOS node (with a versatile device offer), with state-of-the-art SiGe HBT and metallization stacks position B55X as a unique technology in the current BiCMOS landscape. This technology marks a shift in ST roadmap concerning the SiGe HBT architecture and device offer versatility [16]. Next generations will probably follow this trend, keeping an important focus on the balance between performance and complexity. Heterogeneous integration will probably provide interesting perspectives in this respect.

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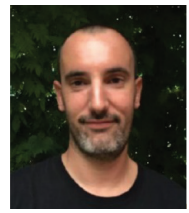

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Claire Deglise-Favre, photograph and biography not available at the time of publication.

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